TDC with Uncontrolled Delay Lines: Calibration Approaches and Precision Improvement Methods

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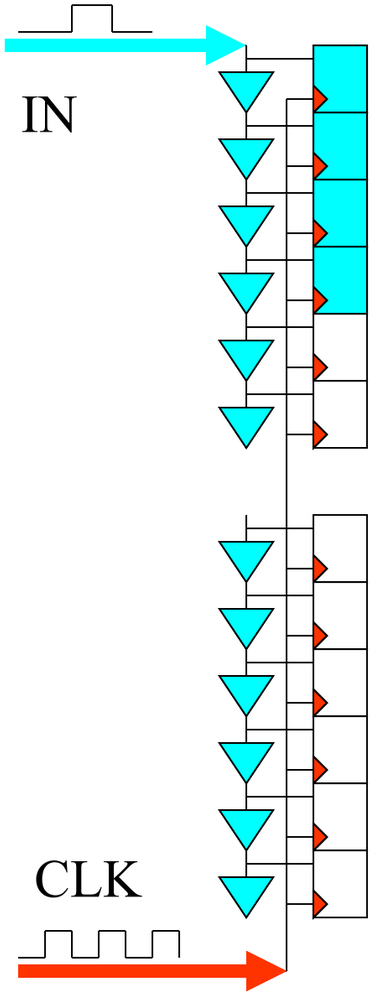
Introduction

- Delay line based TDC was developed in ASIC in 1990's.
- The TDC was transplanted into FPGA in 2000 to 2010 with simplifications with uncontrolled delay line.
- ETROC designed, fabricated and tested in 2018 to 2022 is an attempt of transplanting the simplified TDC with uncontrolled delay line back to ASIC.

TDC with Adjustable Delay Line



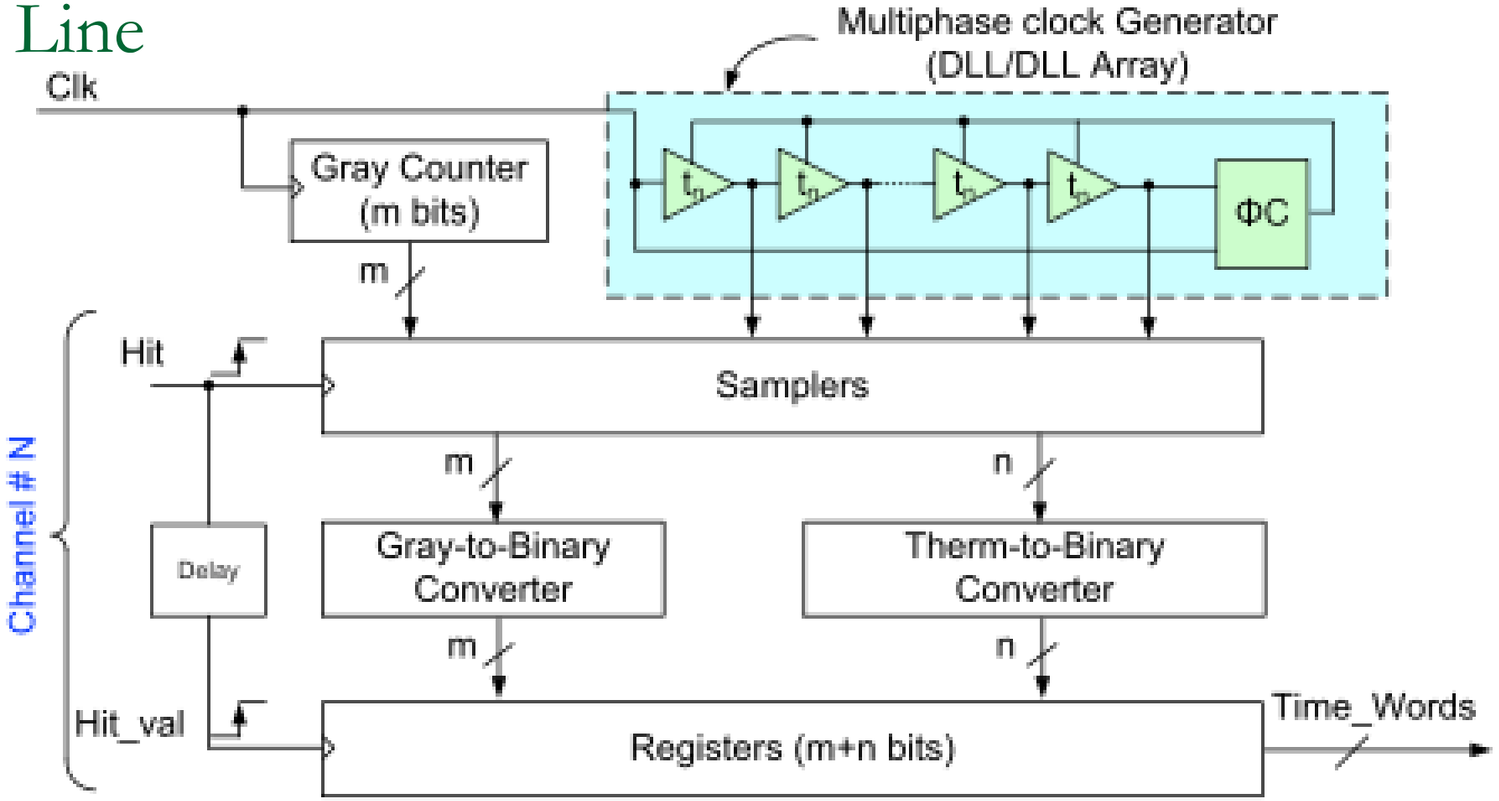
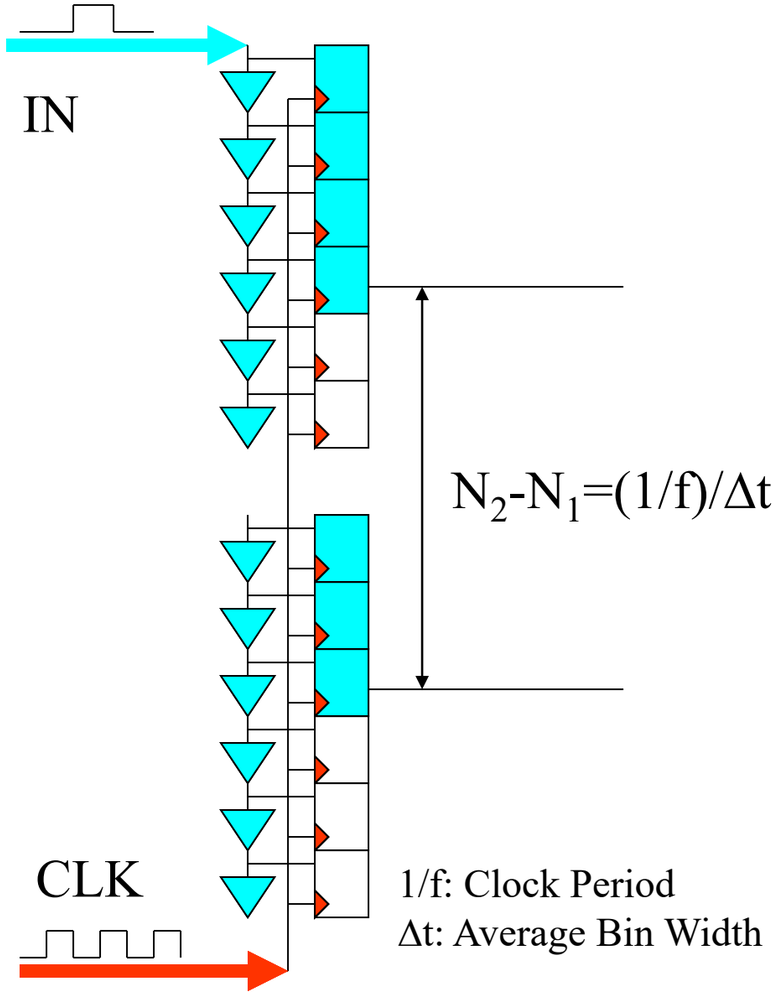
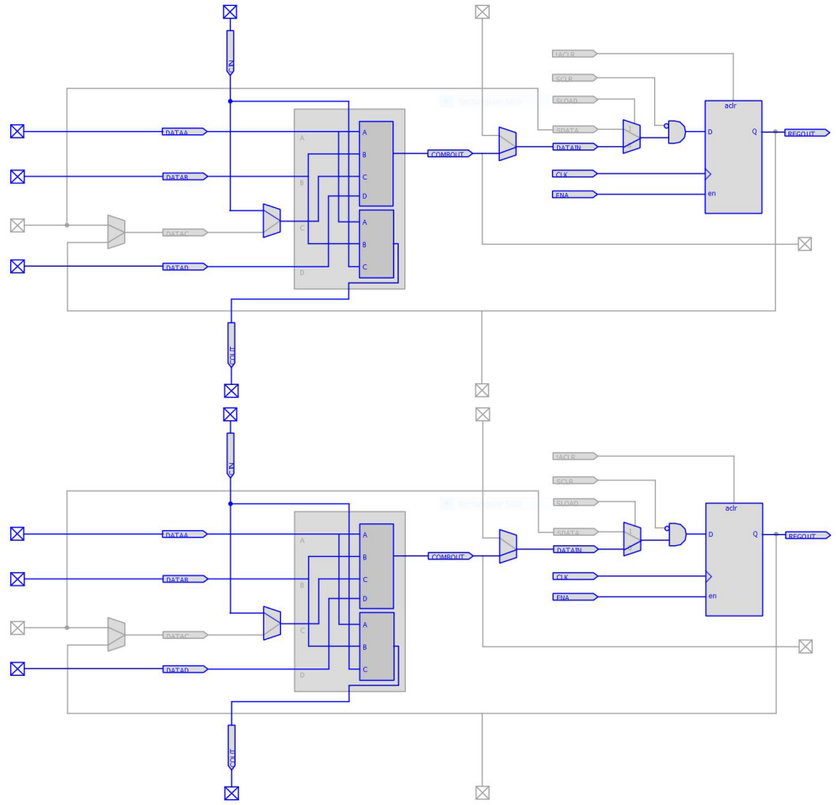


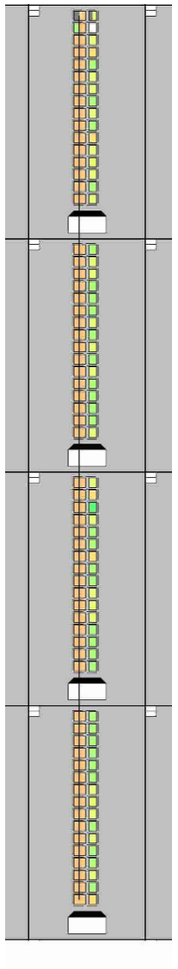
Figure 1: Tranditional architecture of a flash TDC.

- The input signal propagates in the delay chain.
- The "snapshot" is taken into the register array.
- The position of the signal transition is encoded into arrival time relative to the CLK.
- A fast clock (e.g. 320 MHz) is sent to the delay chain.
- The delay cells are adjusted to match the clock period.

Un-adjustable Delay Lines in FPGA

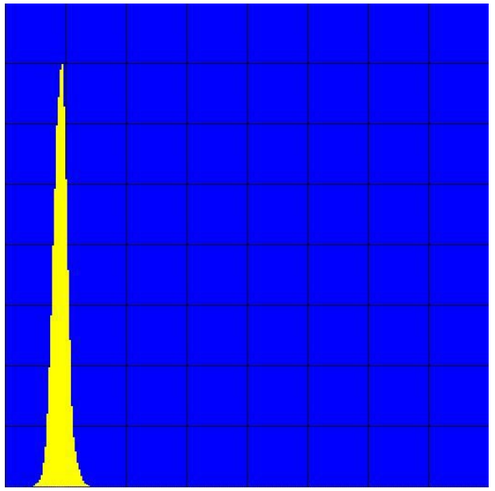


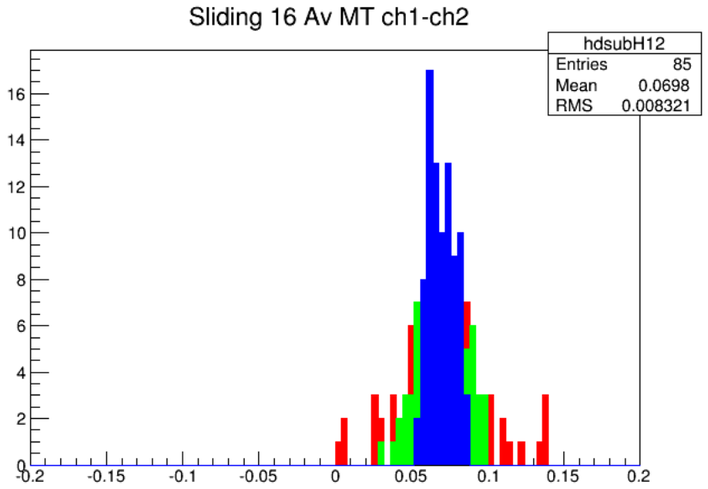


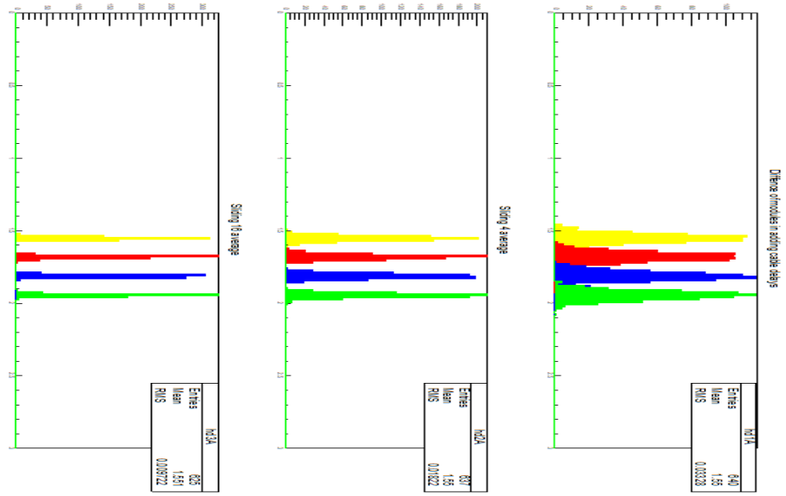


- For each input, make two measurements.
- The extra measurement can be used to calibrate VTC variations.

FPGA TDC

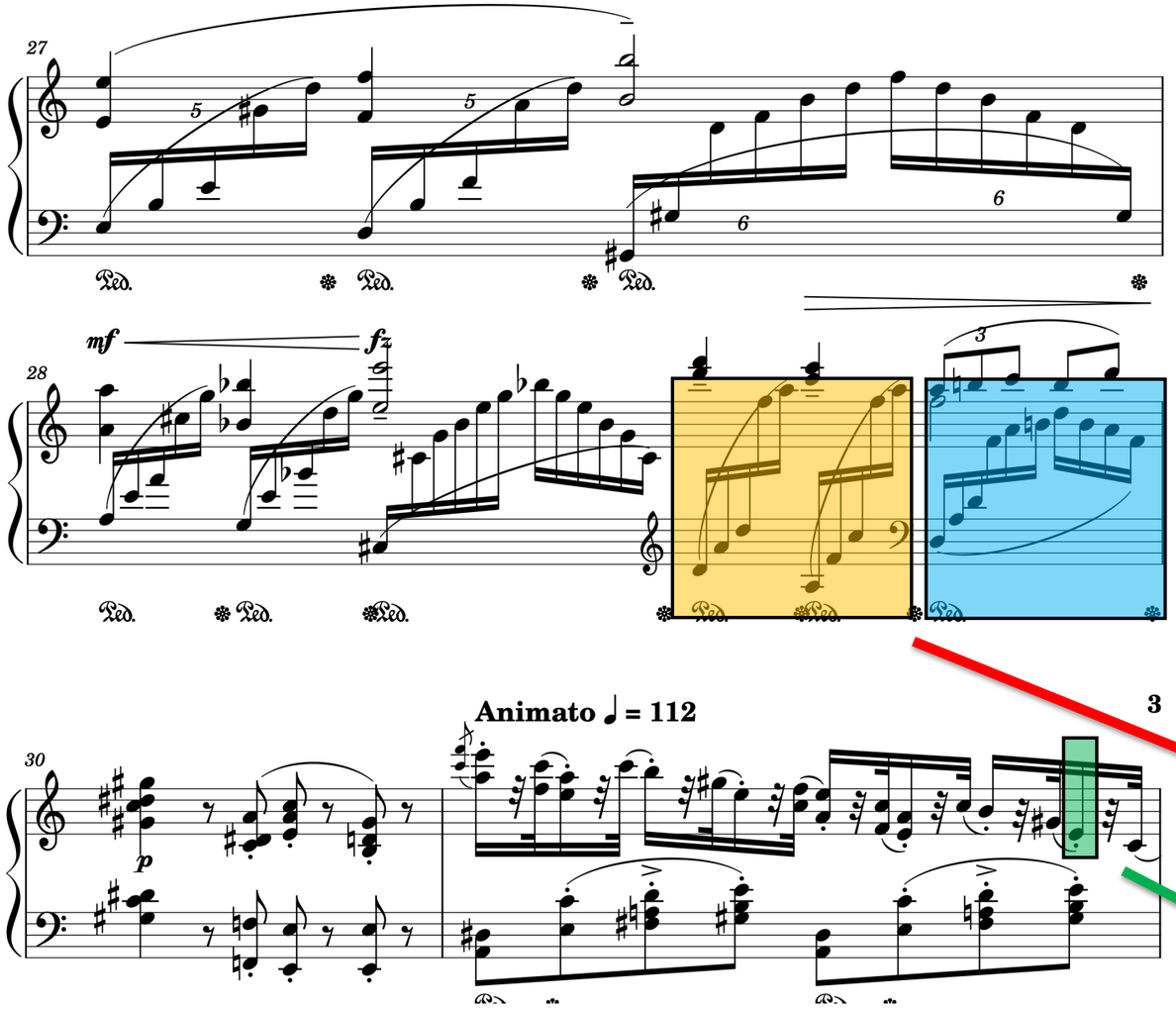


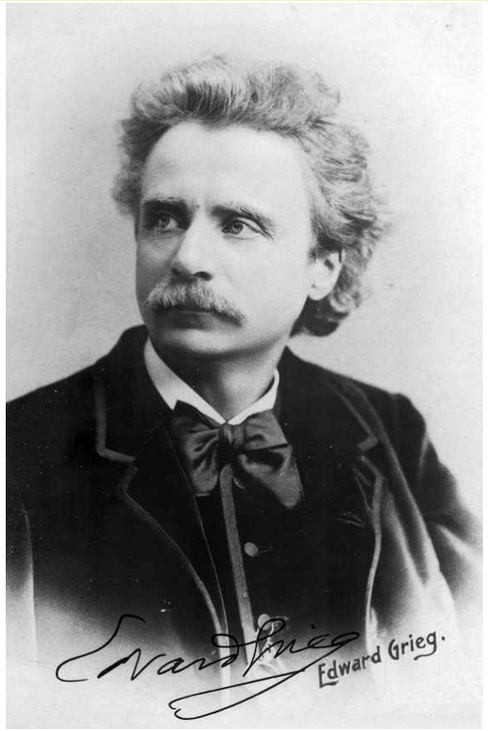




- The delay line is implemented using carry chain inside FPGA.
- Today FPGA TDC precision is better than 20 ps, some high-end ones better than 6 ps.
- It is not necessary to control the delay line speed.

From Edvard Grieg: Piano Concerto, Op. 16





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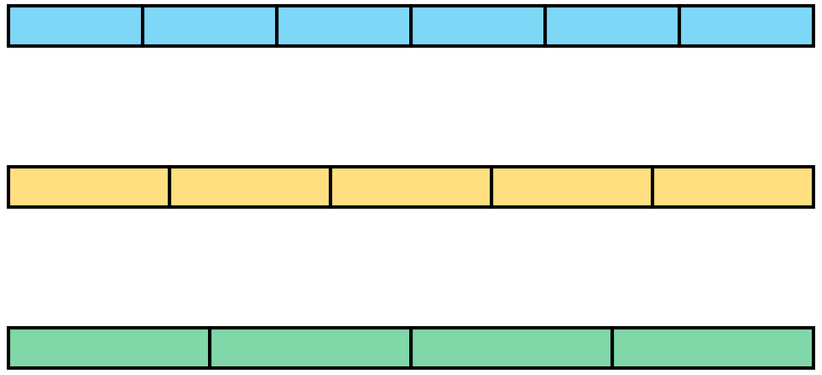
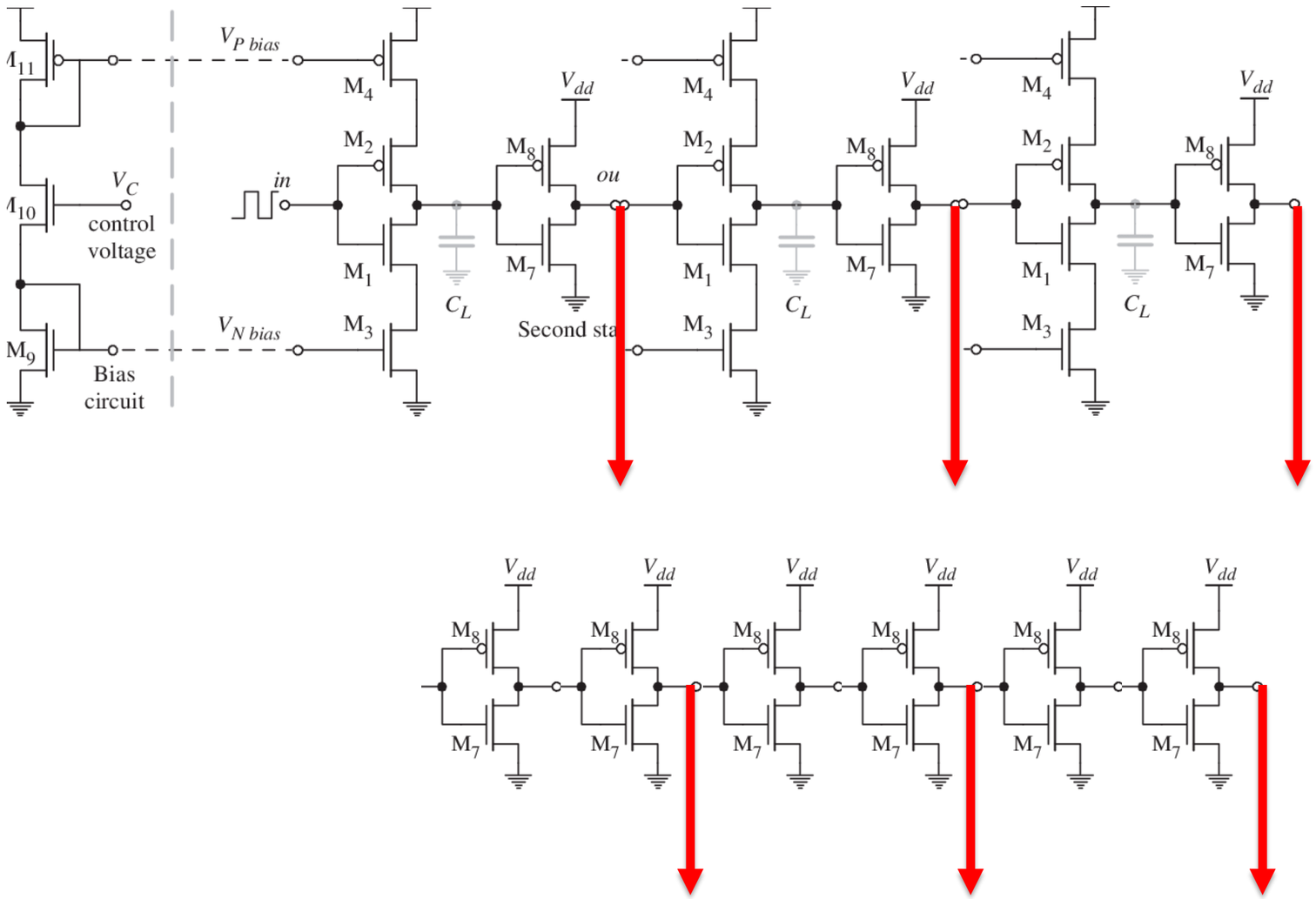


- A beat can be divided into 5, 6 notes, not always 4.

Uncontrolled Delay Line in ASIC TDC

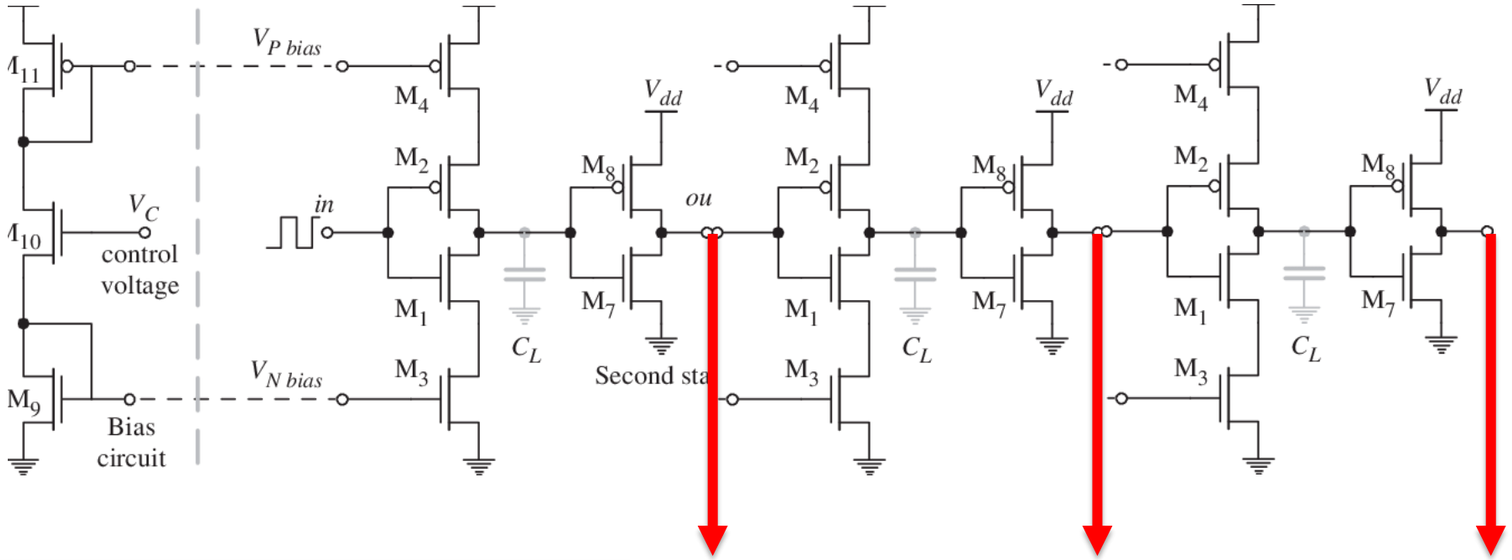
Advantage of TDC with Uncontrolled Delay Line: (1) Full Speed Operation

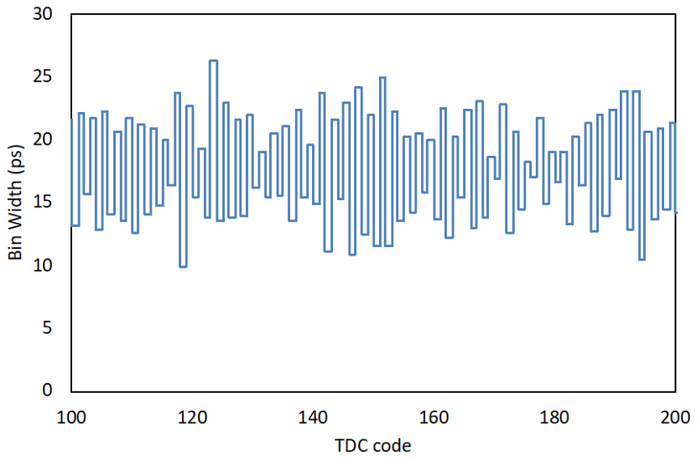


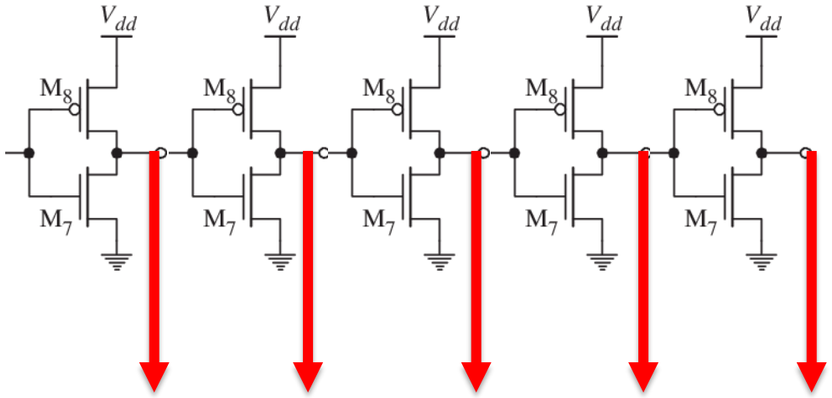
- In controlled delay line, transistors are starved. The delay cell runs slower than in normal condition.

- In uncontrolled delay line, transistors are fully powered. The delay cell runs at full speed.

Advantage of TDC with Uncontrolled Delay Line: (2) Single Gate Delay

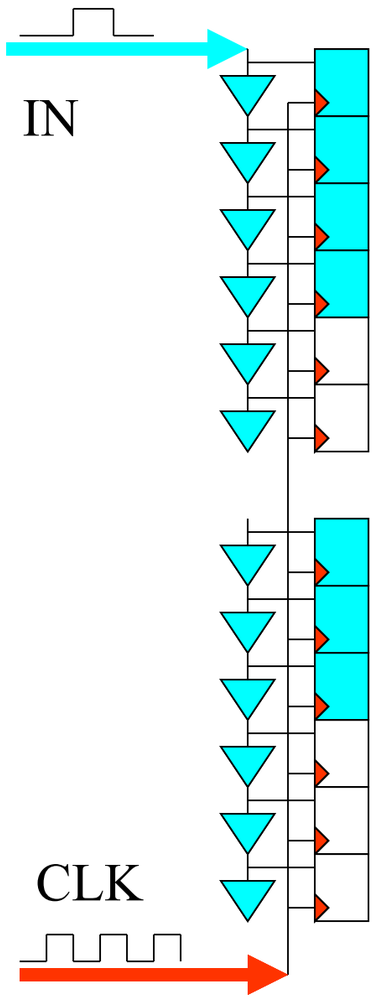


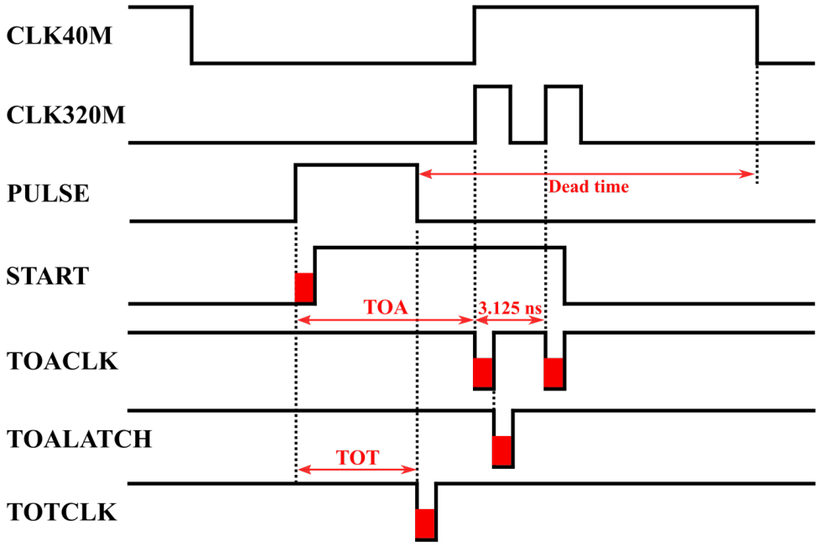


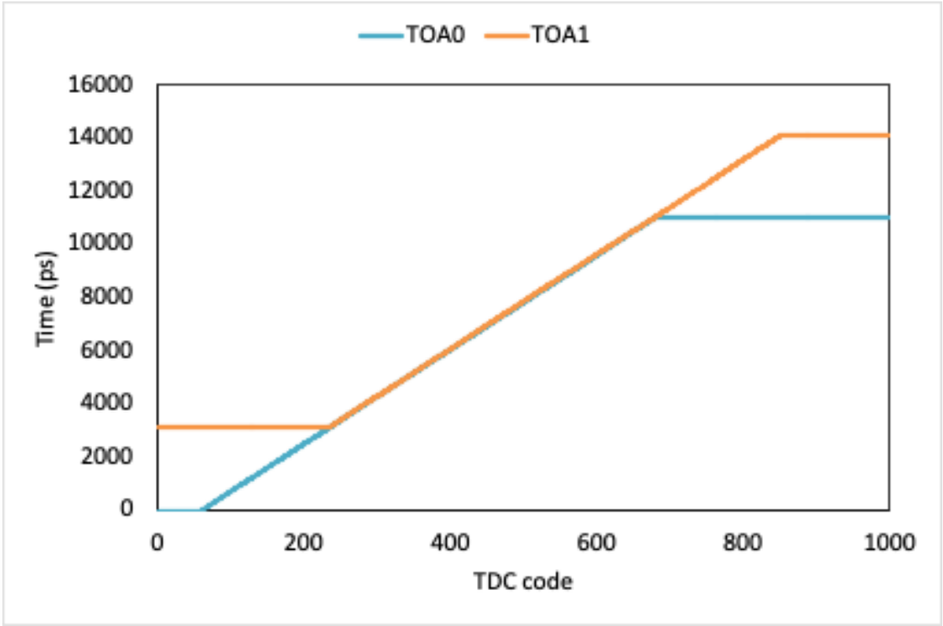


- If even-odd DNL is not tolerated, at least TWO invertor delays are needed between delay taps.
- If DNL can be calibrated, delay between taps can be just a SINGLE invertor delay.

Advantage of TDC with Uncontrolled Delay Line: (3)Multiple Measurements

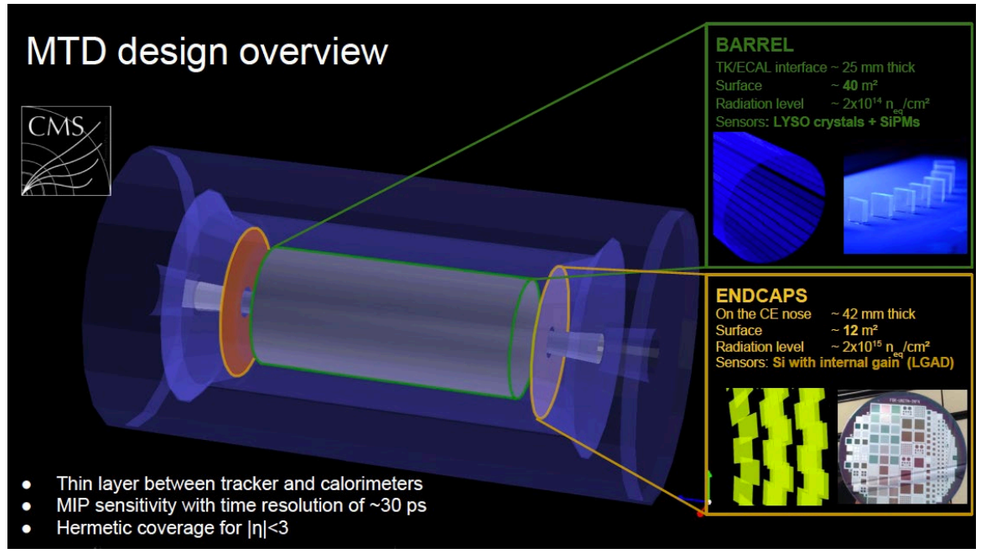


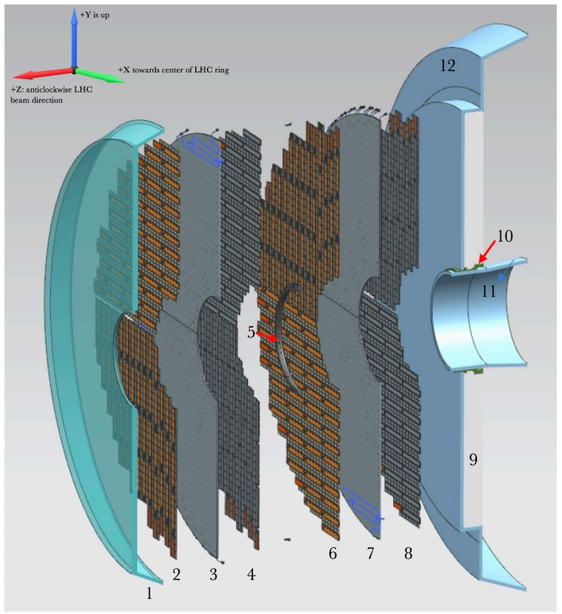




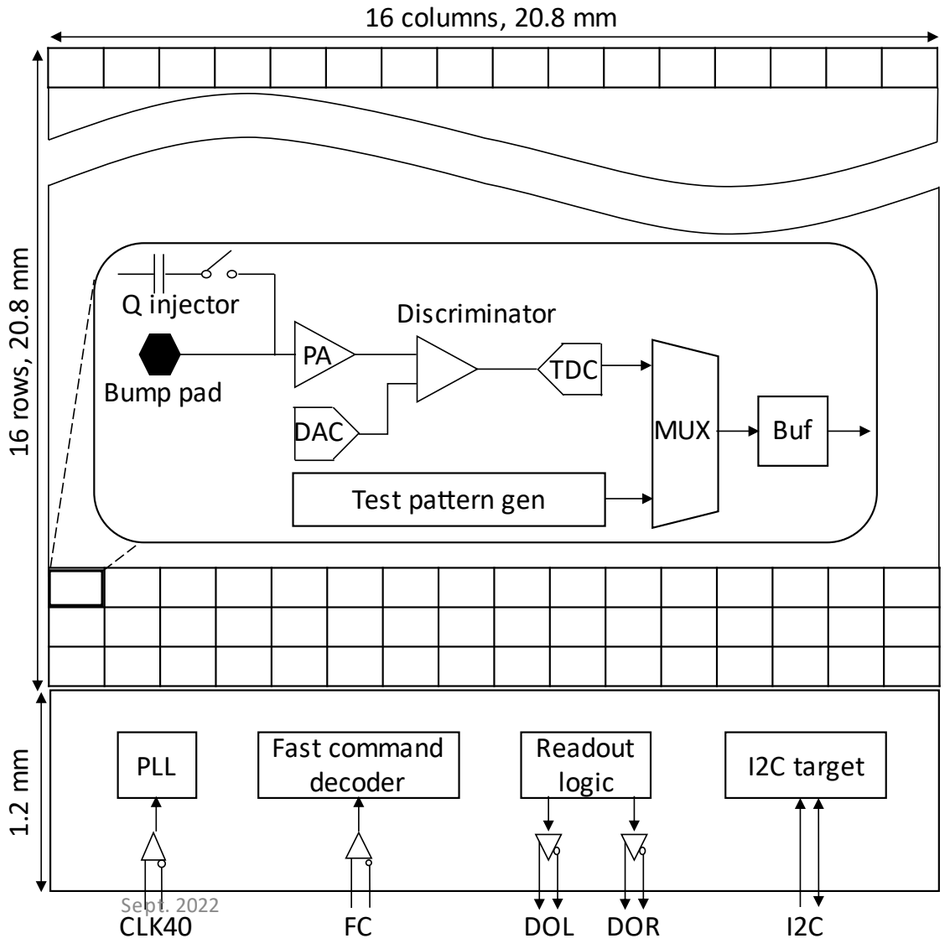
- The TDC with uncontrolled delay line usually needs two measurements for each hit.
- The two data samples can be used for temperature tracking and calibration.
- The two samples can also be averaged for a finer precision.

TDC in End Cap Timing Read Out Chip (ETROC)



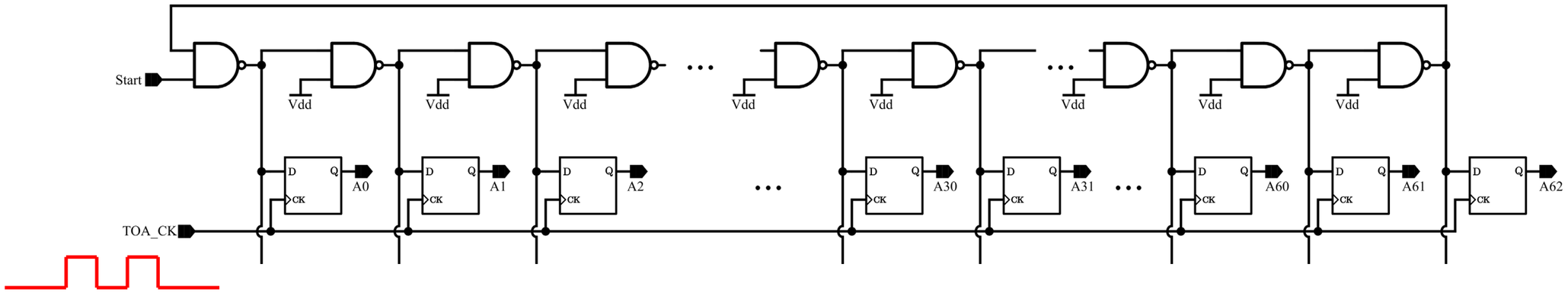


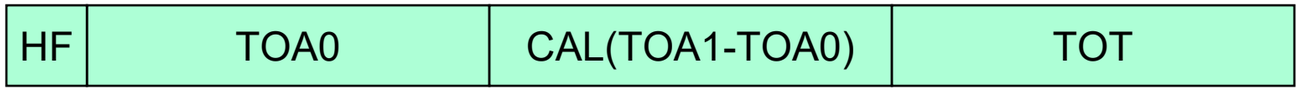
1: ETL Thermal Screen
2: Disk 1, Face 1
3: Disk 1 Support Plate
4: Disk 1, Face 2
5: ETL Mounting Bracket
6: Disk 2, Face 1
7: Disk 2 Support Plate
8: Disk 2, Face 2
9: HGCal Neutron Moderator
10: ETL Support Cone
11: Support cone insulation
12: HGCal Thermal Screen



- The ETROC ASIC interfaces 16 x 16 = 256 pixels.
- The arrival time and pulse width of each hit are digitized with a TDC.

ETROC TDC: Transplanting Uncontrolled Delay Line Back to ASIC TDC

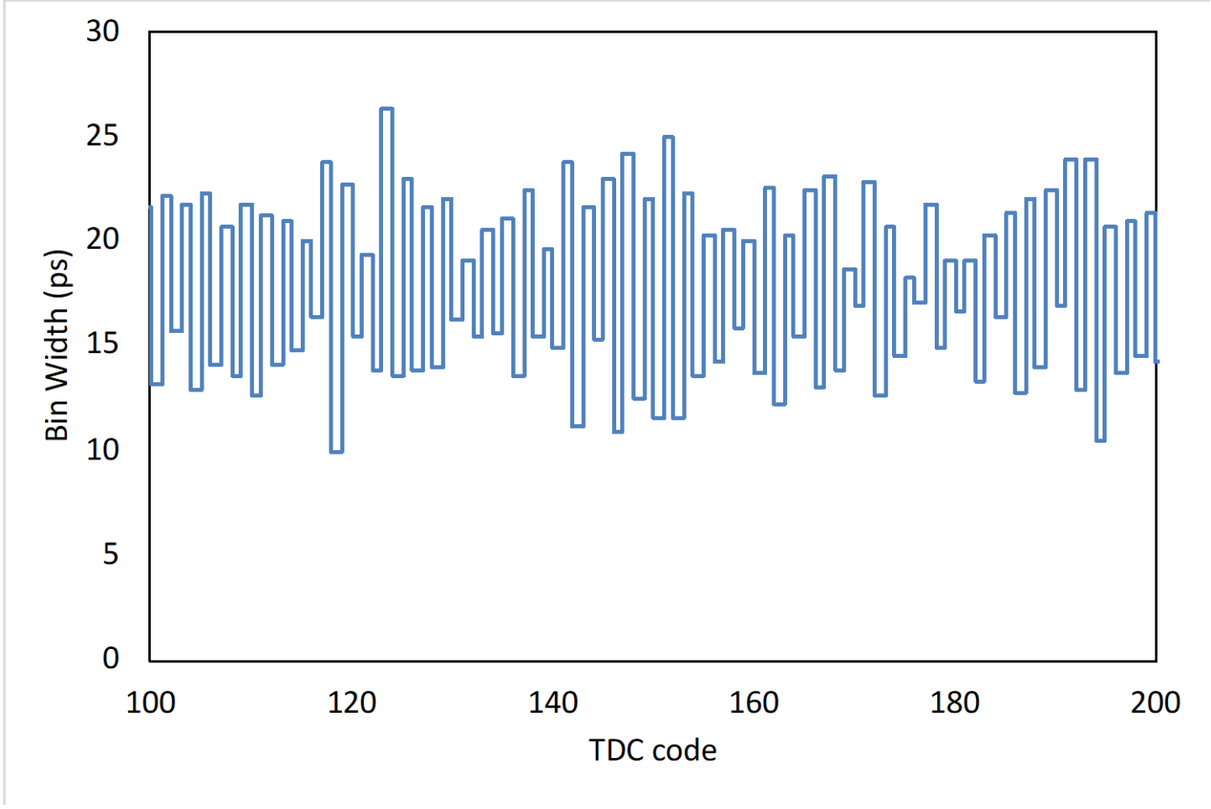




Hit Flag | Time Of Arrival | Calibration Code | Time Over Threshold

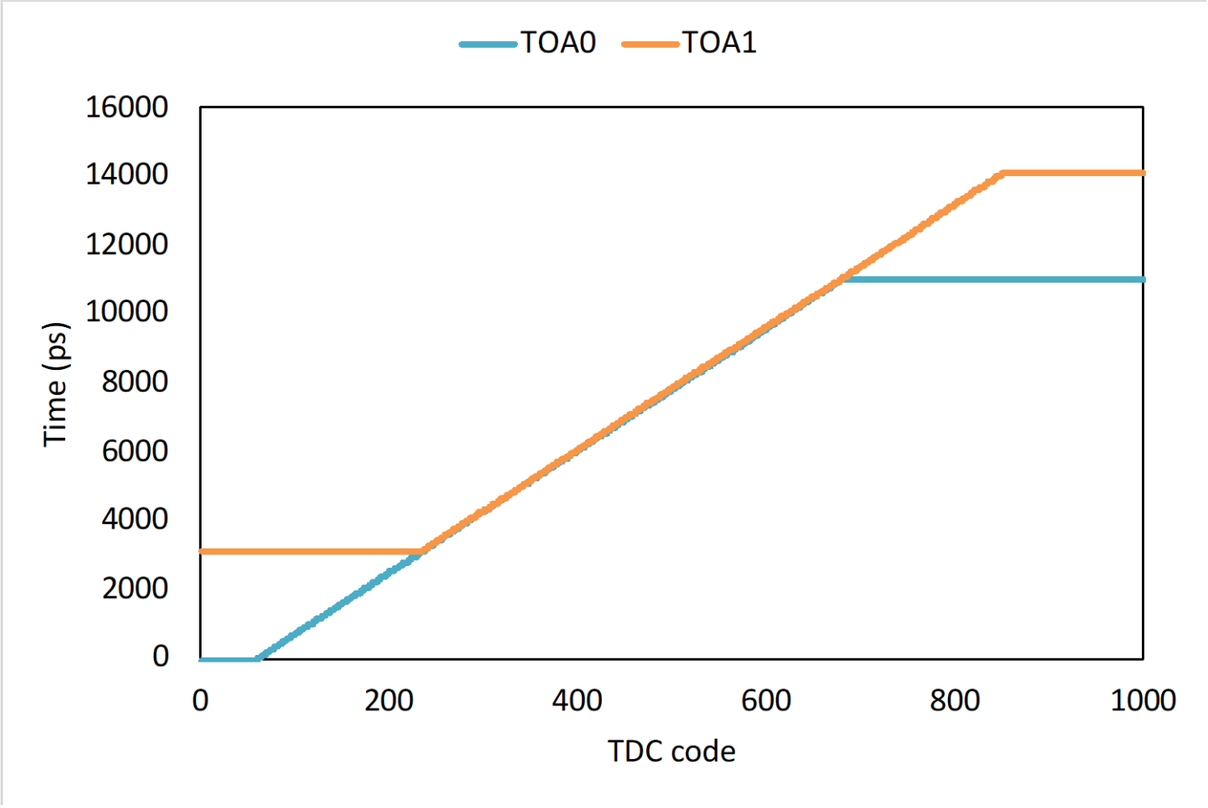
- The delay chain is not controlled so that it runs at full speed.
- Temperature variations and uneven width of the bins are corrected in digital domain.
- Two samples also help improving measurement precision.
- Note that the delay cells are inverting NAND gates with single gate delay (17 ps in 65 nm Technology).
- No hit no flip: very low power consumption.

Bin Widths



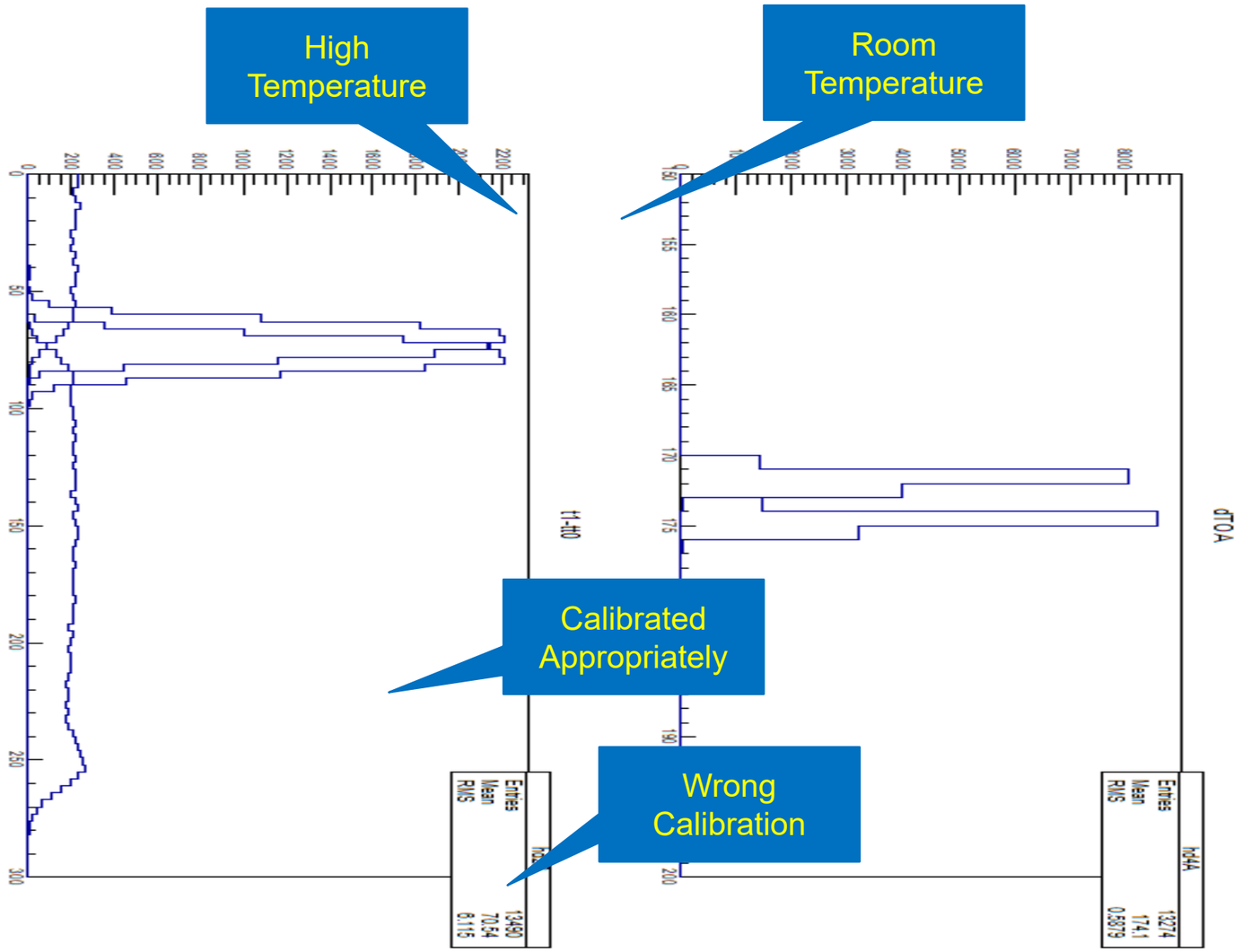
- Bin widths is measured using two clocks generated using PLL with slow drift phase relationship:
  - System clock: 40.000 MHz
  - Test hit generation: 40.001 MHz
- The relative phase drift between system clock and test hits is 0.625 ps per step.
- DNL of even-odd bins can be measured at certain temperature.

Calibration Table



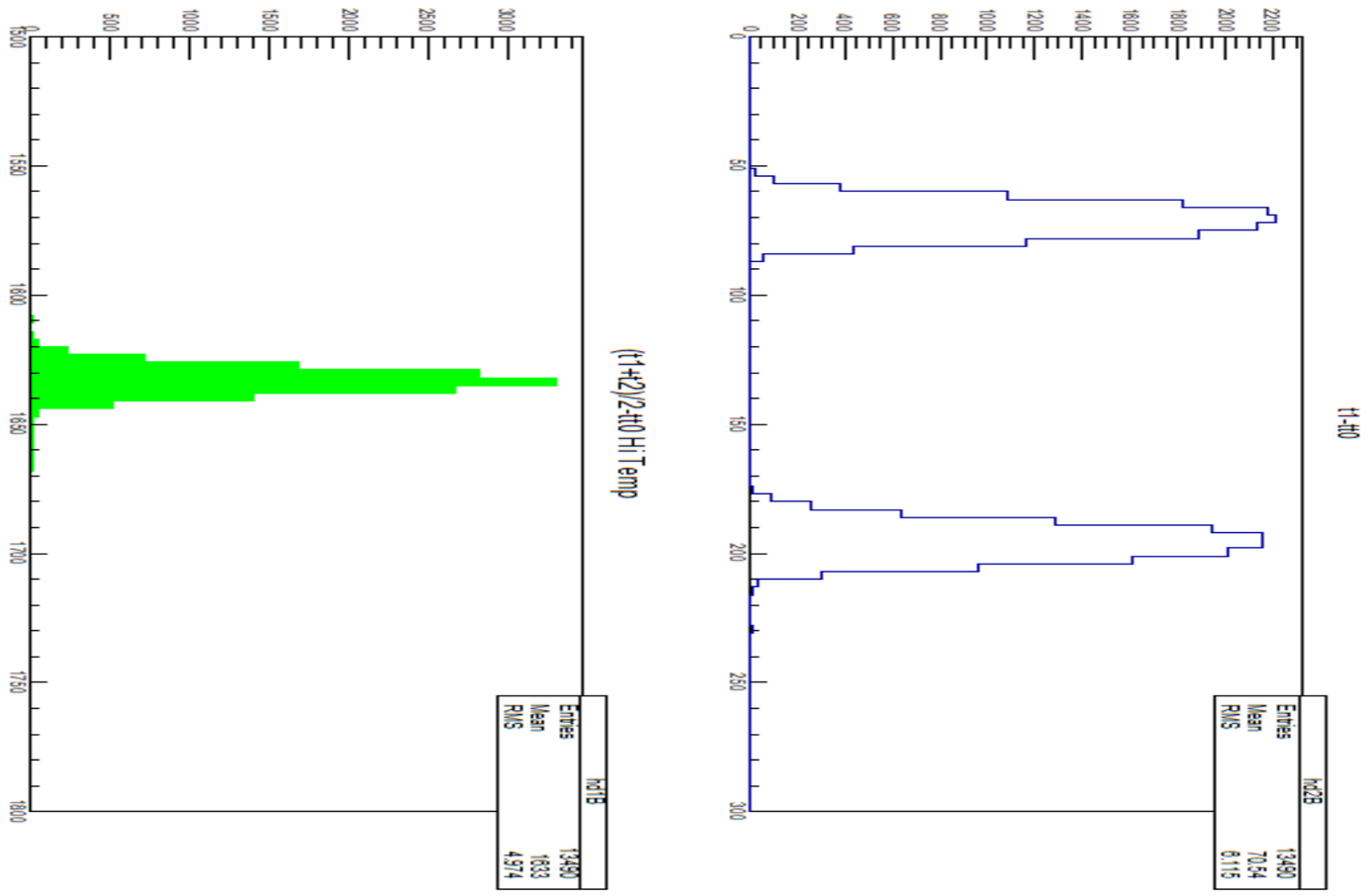
- For each hit, two time of arrival are measured and output as two TDC codes.
- Using the bin width data, two calibration tables for both TDC codes can be accumulated.
- The TDC codes are converted into time (in unit of ps) using the calibration table.

Effects of Temperature Variations



- Measurements are performed on an ETROC TDC at two different temperatures, one at room temperature (about 25 degree C) and another at a higher temperature (heated with a hot air gun to about 40 degree C).
- A very notable phenomenon is the shift of the calibration code, TOA1-TOA0 (dTOA).
- If calibrated correctly, fine measurement precision (~6 ps) can be achieved.
- If calibrated wrong, incorrect results are seen.

Arithmetic Average of Two Measurements



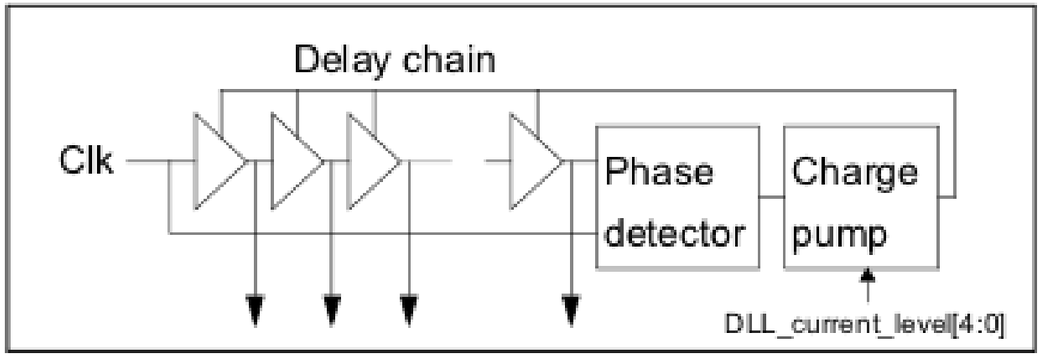
- The standard deviation of two measurements in this situation is about 6 ps.
- When an arithmetic average is calculated for each hit, the standard deviation improves to better than 5 ps.

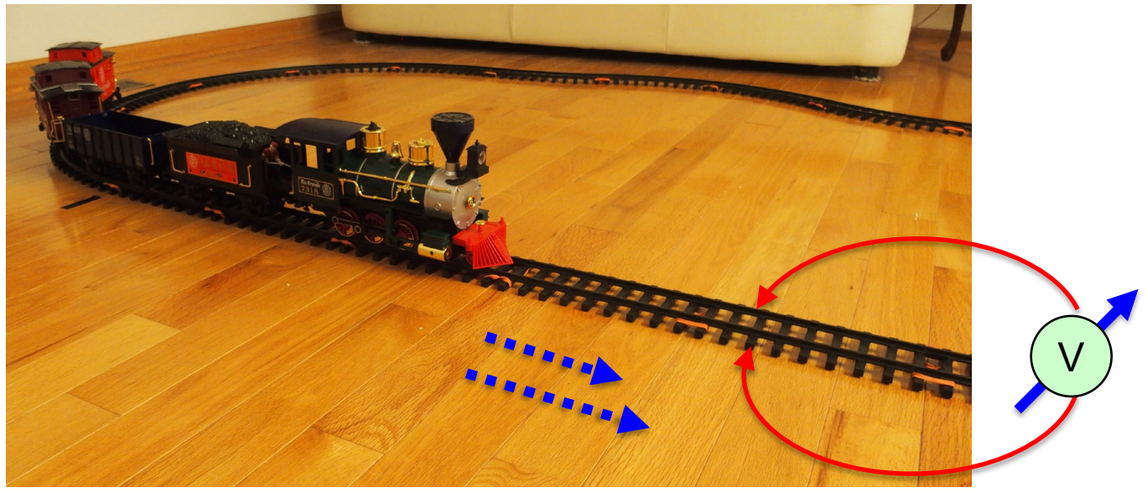
Summary

- Without controlling the delay line, the TDC structure is simpler, and the power consumption is reduced.
- In the TDC with uncontrolled delay line, single invertor at full speed minimize tap delay allowed by the ASIC fabrication technology, resulting finer bin width.
- Extra measurements in double-strobe scheme are not wasted. They are averaged for finer measurement precisions.


The End
Thanks

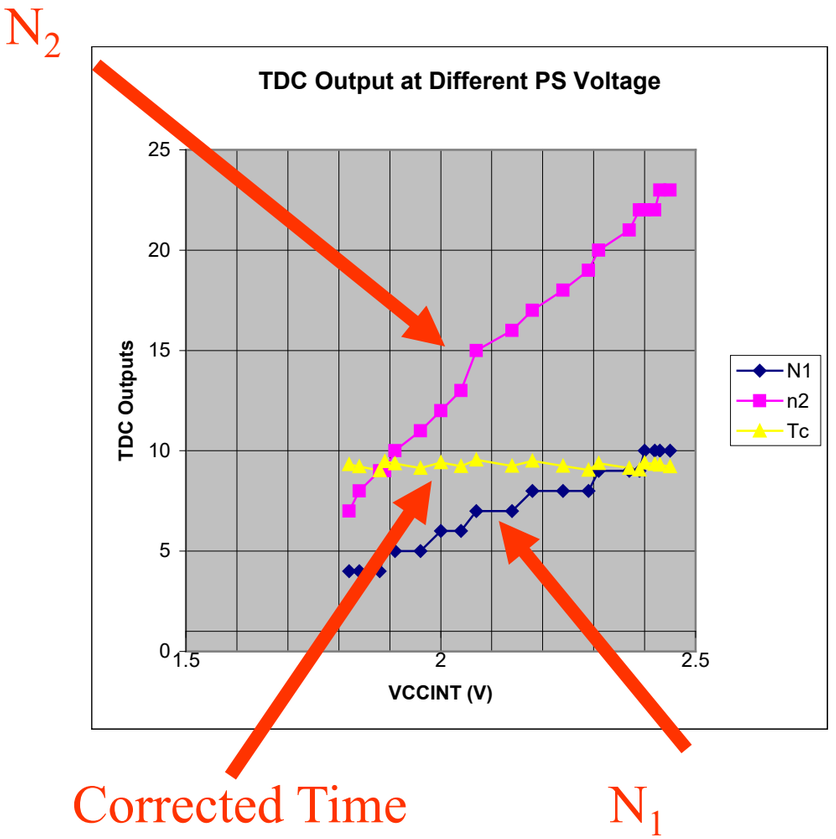
Good Things in ASIC But Not in FPGA





- The phase detector, charge pump and voltage-controlled delay cells are available in ASIC but difficult to implement in FPGA.
- Pro:
  - The delay cells are adjusted to a known speed. (e.g., 100 ps/tap)
- Con:
  - The delay cells are slowed down, rather than running at the full speed.
  - Charge pump consumes extra power.
  - Delay chain must always run.

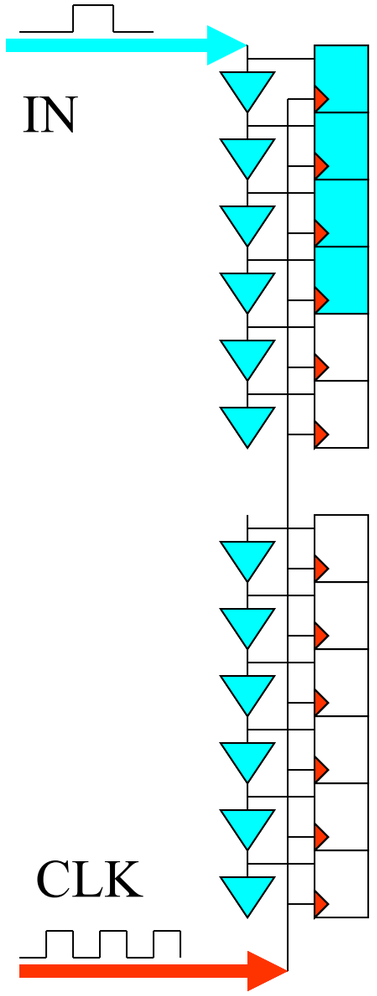
Temperature and Power Supply Voltage Calibration

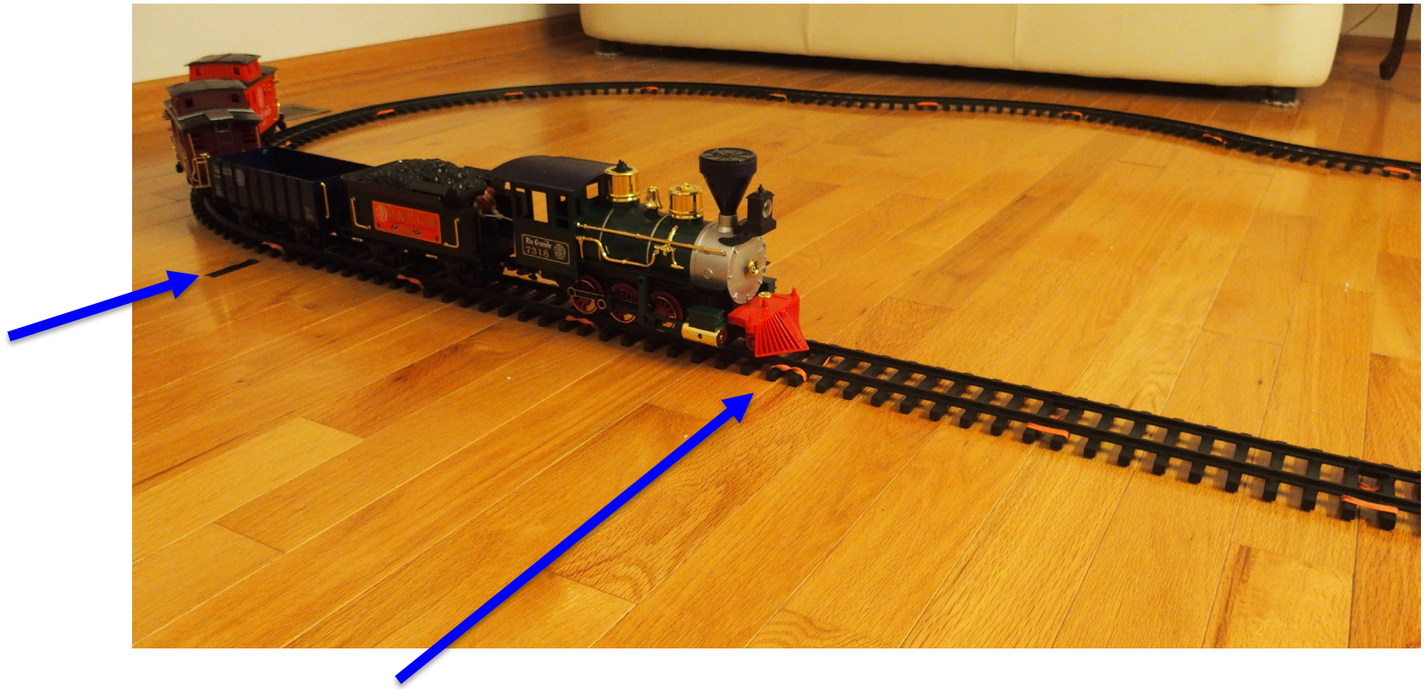


- Temperature and power supply voltage will cause the delay cell speed change.
- With multiple measurements, the variation can be corrected.
- The delay cell always run at full speed rather than being slowed down.

$$T_c = T\frac{(N_1 + N_0)}{\langle N_2 - N_1 \rangle} = \frac{T}{L}(N_1 + N_0)$$

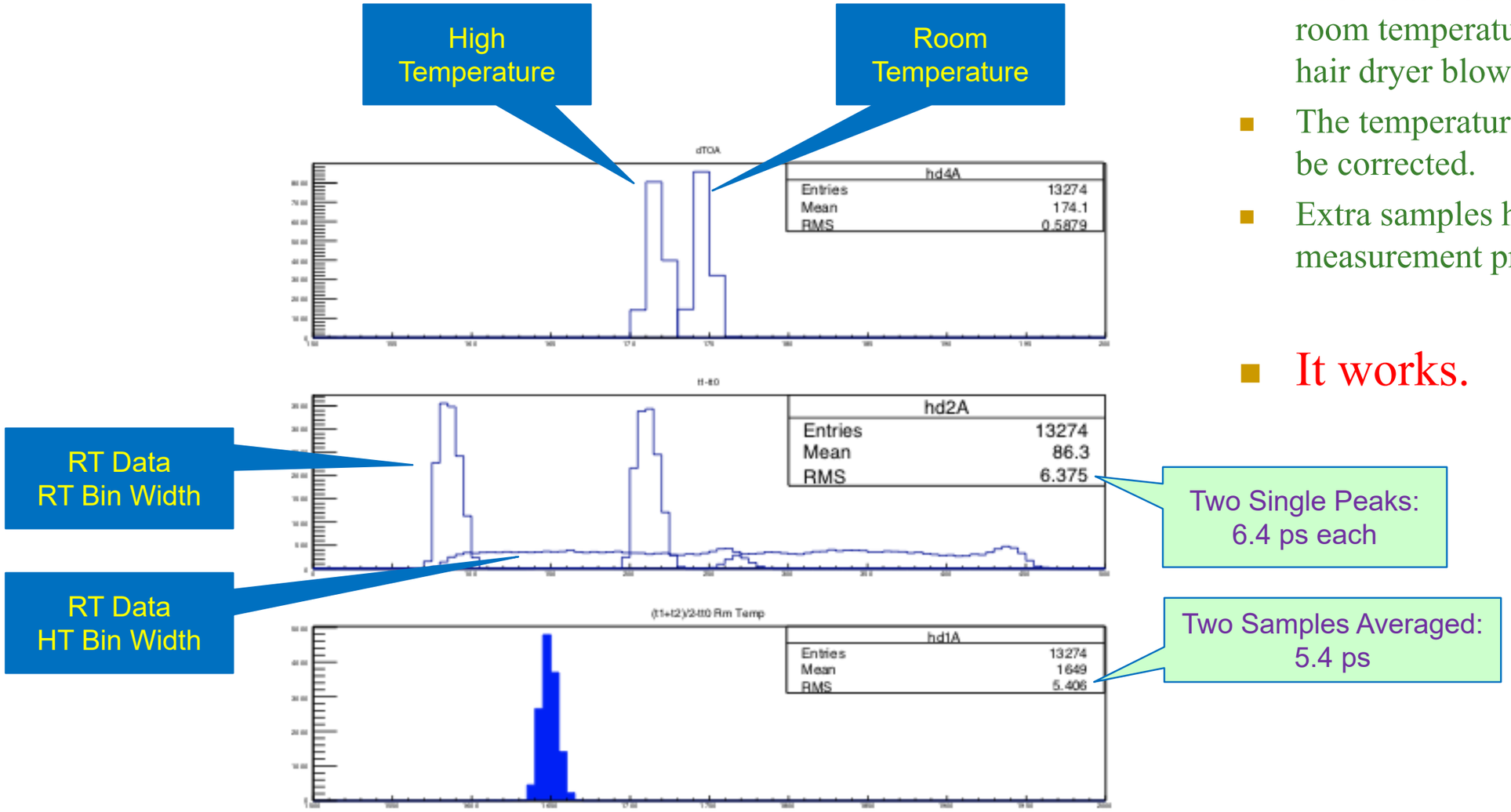
Delay Line Based TDC





- The input signal propagates in the delay chain.
- The “snapshot” is taken into the register array.
- The position of the signal transition is encoded into arrival time relative to the CLK.

Histogram



- The measurements are taken at room temperature and under hair dryer blow.
- The temperature variation can be corrected.
- Extra samples helps improving measurement precision.

- It works.

Mainstream ASIC TDC in History (& Today)

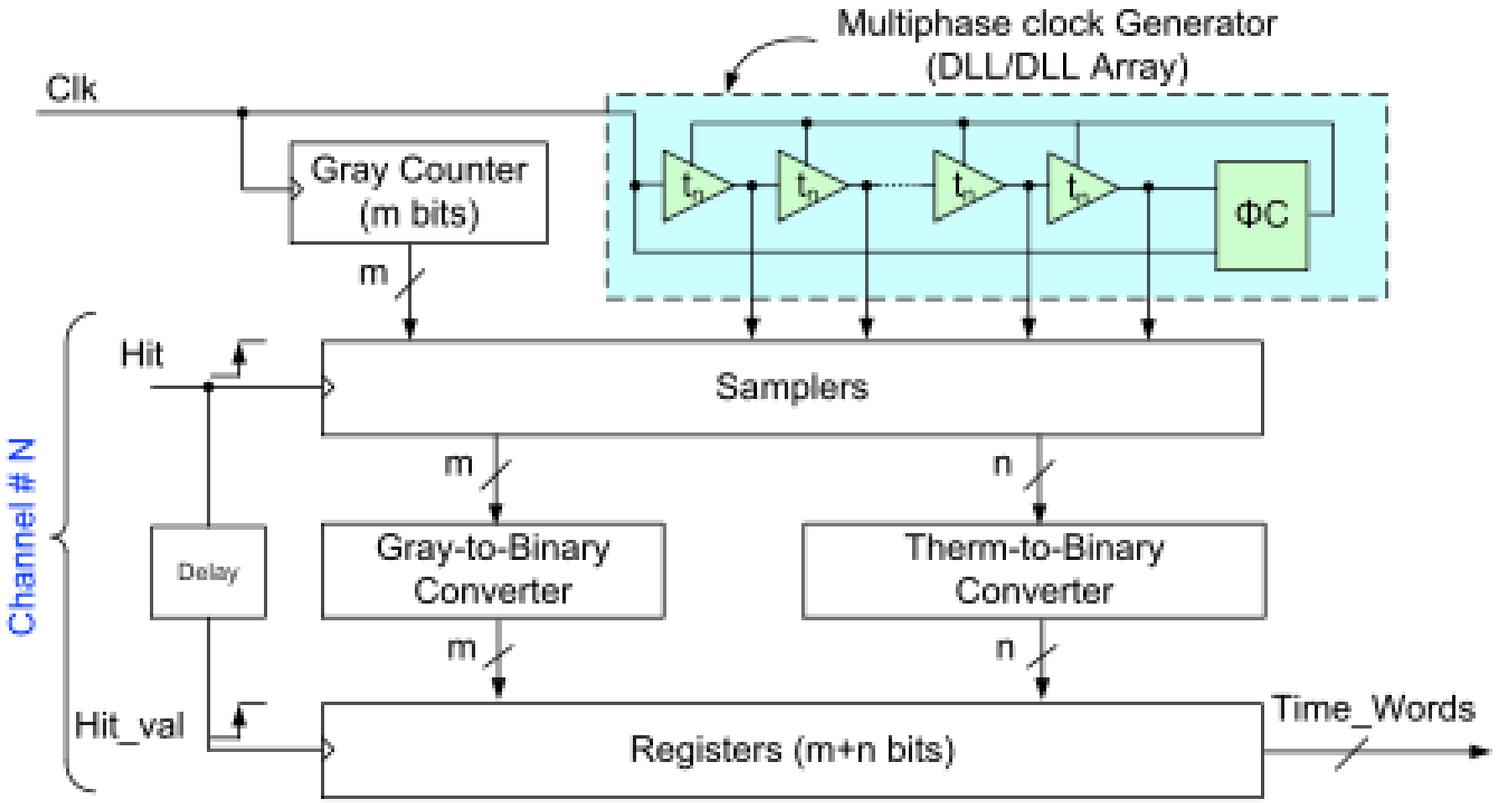
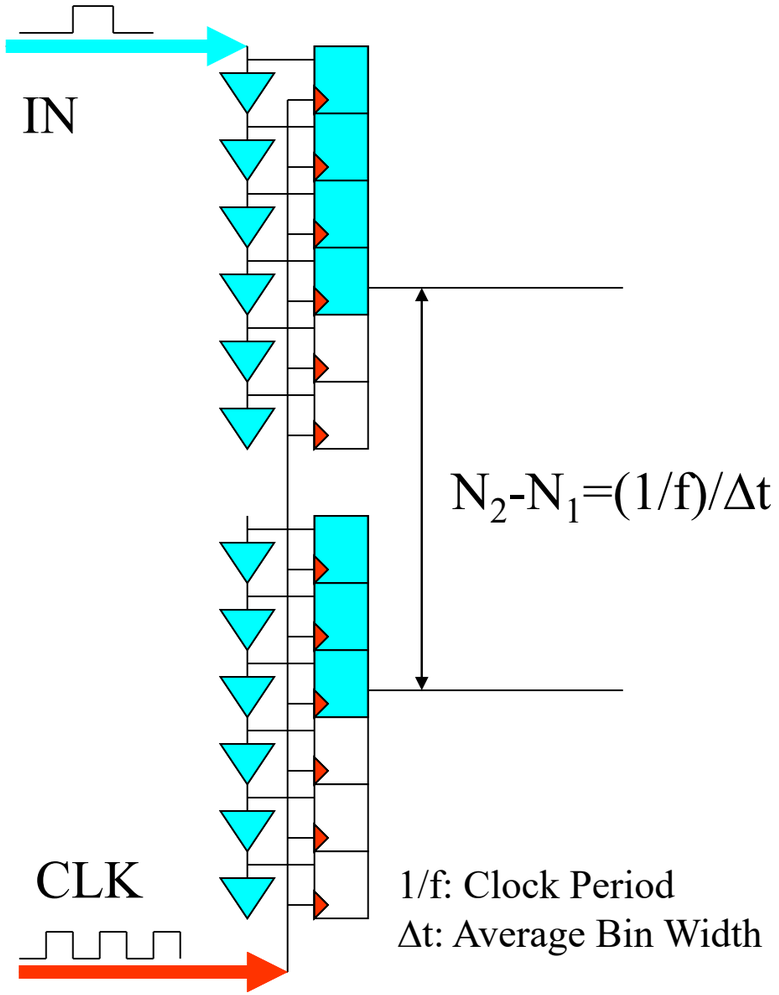
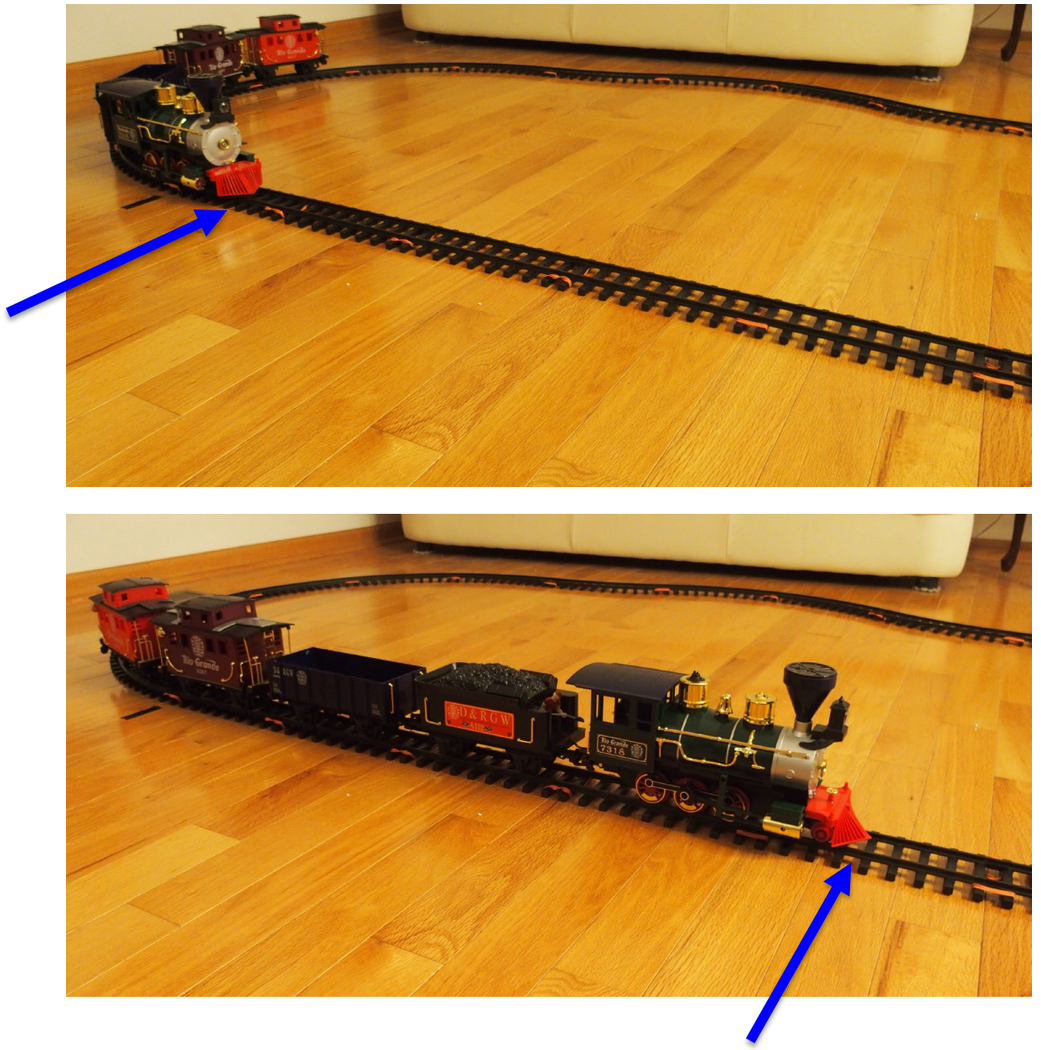


Figure 1: Tranditional architecture of a flash TDC.

- A fast clock (e.g. 320 MHz) is sent to the delay chain.
- The delay cells are adjusted to match the clock period.
- The outputs of the delay taps are routed to a set of FF registers.
- The leading edge of the HIT signal captures the delay pattern.

Un-adjustable Delay Lines FPGA





- For each input, make two measurements.
- The extra measurement can be used to calibrate temperature variation as well as increase measurement precession.