# Study of Alternative Serial Powering Systems for the Future ILC Tracker

M.Turqueti, R.Rivera, J.Chramowicz and A.Prosser

*Abstract*– **The International Linear Accelerator (ILC) is the currently proposed electron-positron linear collider to complement the proton-proton Large Hadron Collider (LHC) located at CERN.**
**One of the main problems foreseen for the ILC detectors is the need for a low material budged on the interaction region. Also, due to its foreseen high density electronics on the tracker, a more efficient way of powering the system is required.**
**In this paper we describe a first step for the development of a power system that can fulfill the ILC calls for low mass and low power. Initially a basic mathematic model of the problem is introduced followed by the description of a proposed system test concept.**

## I. Introduction

This work has as goal to study different powering skins for the vertex tracker based on the serial powering technique as well as hybrid of serial and parallel powering systems.
A test circuit board with a configurable hybrid powering skin will be built in order to investigate the different options. The test board will use the pixel readout chip FPIX2.1 [1] as test device. Also, the power lines were used as data communication medium and then connected to the pixel chip and used to program the chip.
The main objective of this work is to compare the performance of the multiple powering skins here presented, as well as to provide results on the viability of the use of the power line as a communication line. Also is a goal of this work to introduce a initial mathematical models in order to better understand the challenges involving this kind of powering.

Serial power applied to high energy physics has as main objective to reduce the material budget in the interaction area. It does so by removing the massive amount of cables required to power the detector electronics and exchange it by a chain-like power grid. While serial power is capable of reducing the material budget, it is inherently susceptible to catastrophic system failure. This makes necessary to add security features or a balance between serial and the parallel approach, thus a hybrid powering system.

In order to better understand the basic trade off between the traditional parallel powering and serial powering a mathematical model based on graph theory is presented next.

## II. Mathematical Model

The model presented here will be based on labeled undirect graphs where the edges ($e_n$) of the graph can represent the cabling cost, the line reliability or the power cost and the ordinary vertices ($V_n$) the power supply and load. The load can be for example a pixel detector module. The graph will be expressed as G($V_n$, $e_n$).

The material budget in any of the following systems can be calculated using

$$M = \sum_{i=0}^{n} e_i \qquad (1)$$

Where M is the total cost and $e_n$ the n-edge of the graph.
All the graphs presented here will have two special vertices called source(So) and sink(Si), this vertices represent the anode and the cathode of the power supply.
With this initial introduction the first model will be now introduced.

### A. The Parallel System

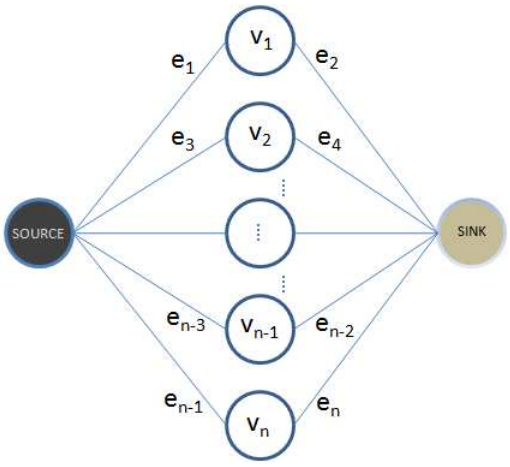


**Fig. 1 The graph representation of the parallel system.**

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The first important thing to notice in this graph is that there is no edges flowing between ordinary vertices, all the edges flow from source to ordinary vertices and from ordinary vertices to the sink. This makes the system to be extremely tolerant to failures, but at the same time very massive.
From the graph shown by Fig. 1 it is possible to extract its adjacency matrix, as

$$Am=\begin{array}{c} \\ So \\ V_1 \\ V_2 \\ \vdots \\ V_{n-1} \\ V_n \\ Si \end{array}\begin{array}{c} \begin{array}{ccccccc} So & V_1 & V_2 & \dots & V_{n-1} & V_n & Si \end{array} \\ \begin{bmatrix} 0 & e_1 & e_3 & & e_{n-3} & e_{n-1} & 0 \\ e_1 & 0 & 0 & \cdots & 0 & 0 & e_2 \\ e_3 & 0 & 0 & & 0 & 0 & e_4 \\ \vdots & \vdots & & \ddots & & \vdots & \\ e_{n-3} & 0 & 0 & & 0 & 0 & e_{n-2} \\ e_{n-1} & 0 & 0 & \cdots & 0 & 0 & e_n \\ 0 & e_2 & e_4 & & e_{n-2} & e_n & 0 \end{bmatrix} \end{array}. \quad (2)$$

All adjacency matrices presented on this paper will be symetric as the graphs are undirect. Also, all the matrices will have the diagonal $d_{i,j}$ with i=j zeroed. This will happen because no graph will have connections to itself.
From the sum of the rows of the lower half of the matrix is possible to obtain the total cost of the graph.
A particullar mark of a exclusivery parallel system is that it will not have edges other than in the columns and rows belonging to the source and sink.
The adjacency matrix is extrimally important so automatic calculation of several parameters of the system can be devised.

### B The Serial System

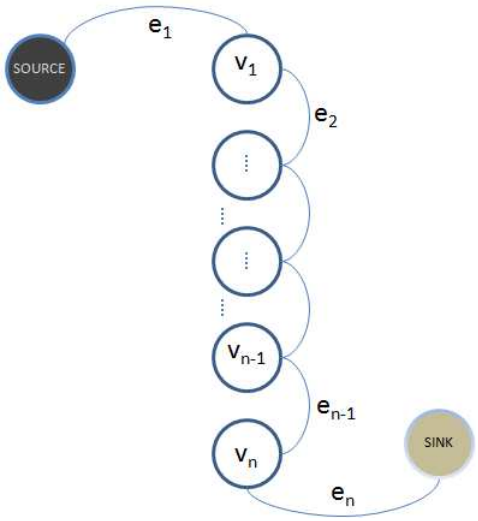


Fig. 2 The serial power system graph representation.

Above, the serial system representation is illustrated. The adjacency matrix can now be extracted, and it is

$$Am=\begin{array}{c} \\ So \\ V_1 \\ V_2 \\ \vdots \\ V_{n-1} \\ V_n \\ Si \end{array}\begin{array}{c} \begin{array}{ccccccc} So & V_1 & V_2 & \dots & V_{n-1} & V_n & Si \end{array} \\ \begin{bmatrix} 0 & e_1 & 0 & & 0 & 0 & 0 \\ e_1 & 0 & e_2 & \cdots & 0 & 0 & 0 \\ 0 & e_2 & 0 & & 0 & 0 & 0 \\ \vdots & \vdots & & \ddots & & \vdots & \\ 0 & 0 & 0 & & 0 & e_{n-1} & 0 \\ 0 & 0 & 0 & \cdots & e_{n-1} & 0 & e_n \\ 0 & 0 & 0 & & 0 & e_n & 0 \end{bmatrix} \end{array}. \quad (3)$$

Here again the graph total cost can be calculated by the summing of the colunms belonging to the lower portion of the matrix. A particularity of the serial adjacency matrix is that all edges exist along the two diagonals neighbors to the main diagonal $d_{i,j}$ with i=j.
The weak point of the serial system is that althouth it will always provide the best material budget, the reliability of the system will be always the worst possible, if one of the components on the system fail the whole system will fail.

### C The Hybrid System

The last system presented here is the hybrid system where there is a mixture between the serial and the parallel systems. Bellow, the graph representation of this system is presented.

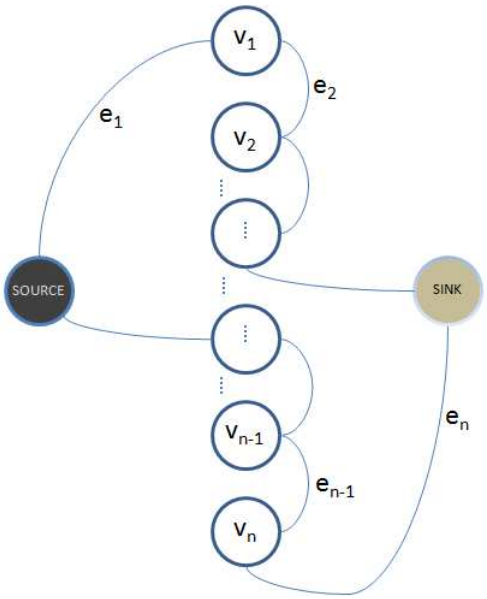


Fig. 3 The hybrid power system graph representation

It is worth to mention that the hybrid system can always be decomposed in a union of disjoint serial and parallel graphs, and so the graph can be expressed in terms of series of serial and parallel adjacency matrices. This sometimes can facilitate the computation needed to obtain certain system parameters, especially when the system complexity is high.

The adjacency matrix of this system is expressed by

$$Am = \begin{array}{c} \\ So \\ V_1 \\ V_2 \\ \vdots \\ V_{n-1} \\ V_n \\ Si \end{array} \begin{array}{c} \begin{array}{ccccccc} So & V_1 & V_2 & \dots & V_{n-1} & V_n & Si \end{array} \\ \begin{bmatrix} 0 & e_1 & 0 & & e_{n-3} & 0 & 0 \\ e_1 & 0 & e_2 & \cdots & 0 & 0 & 0 \\ 0 & e_2 & 0 & & 0 & 0 & 0 \\ & \vdots & & \ddots & & \vdots & \\ e_{n-3} & 0 & 0 & & 0 & e_{n-1} & 0 \\ 0 & 0 & 0 & \cdots & e_{n-1} & 0 & e_n \\ 0 & 0 & 0 & & 0 & e_n & 0 \end{bmatrix} \end{array} . \quad (4)$$

It is clear by observing the features of this matrix that it is composed by both serial and parallel components.
The cost of the hybrid adjacency matrix can be expressed in the same fashion as the later two.
The hybrid system is the most promising approach in order to obtain an optimum balance between material budget and reliability were the goal of the designer between material versus reliability can be calculated.

## III. The Proposed Test Structures

Now that a comparative overview of the possible theoretical implementations was presented, a real implementation taking in account technological factors is proposed.
Assuming that a hybrid solution is the best approach, a basic test topology is proposed were there are basically four different blocks that can be tested and changed by different implementations.
These blocks can be exchanged by block of similar function but different implementation.
The first block is block A and it can be observed on Fig. 4, it is basically a high pass filter to allow the communication signal to pass through the shunt regulator. This block also works as a bypass system in case one of the circuits of this section fail it will bypass the section.
A section is composed by blocks A,B,C and D plus its load(u1), u1 is the system that it is being powering, eg: pixel module.
Block B is basically a power transference block, it transfer power from the serial network to the detector subsystem. This block can be implemented by a diode, a shunt regulator or an air core transformer.

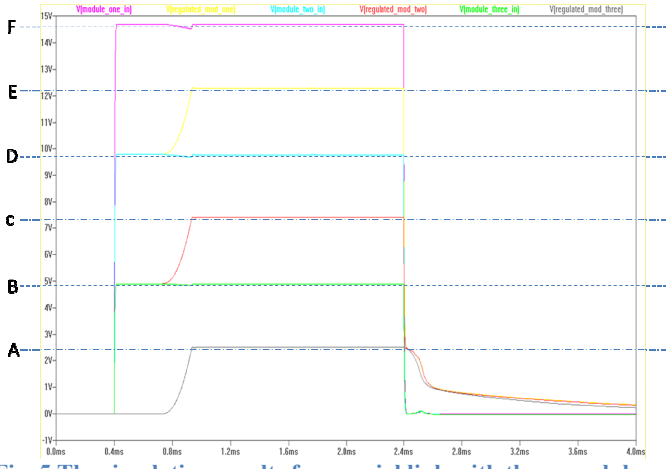


**Fig. 5 The simulation results for a serial link with three modules.**

The next block is block C and it is used for communication, the main idea here is to receive and demodulate the data coming from the power supply. This block will be better explained in the next section.
Finally, block D is the last block and it implements the voltage regulation for the module wish it is powering. This block can be implemented basically in two ways, by a very low drop high efficiency linear voltage regulator or by a high efficiency capacitor switched voltage regulator. A third possibility is to use PWM regulators with air coil inductors.
All this blocks are implemented as separately pluggable PCBs

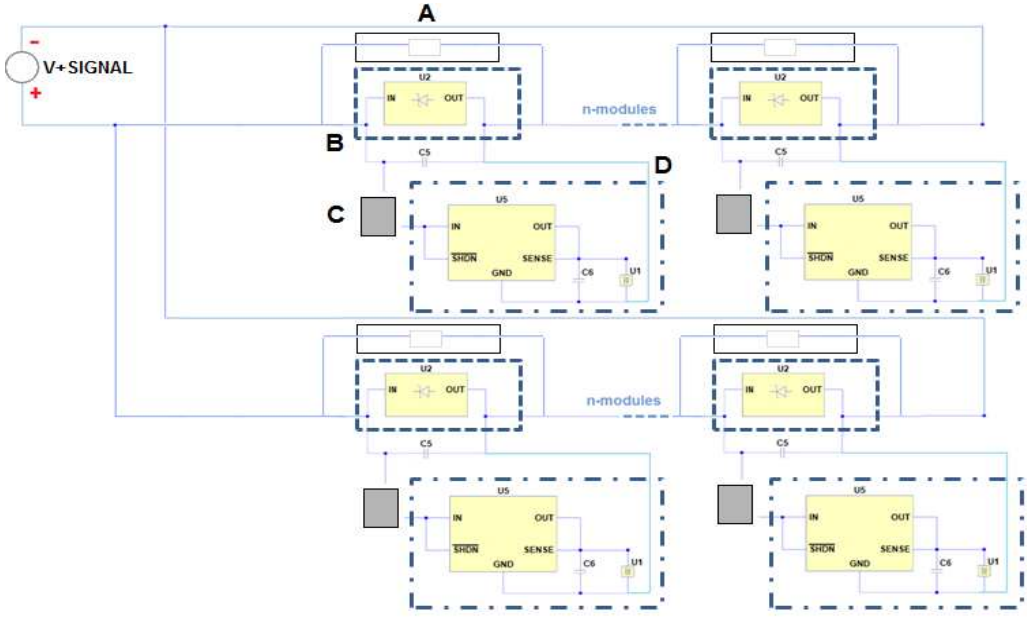


**Fig. 4 The proposed test topology.**

and they can all be plugged in the mother board that is mainly a passive board with sockets for the blocks and with the load that in the case of this test circuit will be a pixel detector.
The system will be able to operate in DC and pulsed mode.
Currently only simulations were performed on the diverse possible block combination, consequently results such as noise effects on the pixel detectors are still inexistent.
Analysis from the simulations suggests that the best choice in terms of efficiency is to use linear regulators if there is more than 3W per serial link. On another hand if less than 3W are required, the capacitor switched voltage regulator is the best choice.
Fig. 5 shows the simulation result of a serial link with three modules where A and B are the first module, C and D the second and E and F the third. B,D and F is the unregulated power arriving to the modules while A,C and E are the regulated power for the respective pixels. The topology of this simulation is similar with the serial branch of the topology shown in Fig. 4.

## IV. Communications Over Power Lines

Power over data lines is already a reality for domestic users, Broadband over Power lines or (BPL) is currently being test in many countries. There are reports of USB systems over power lines transmitting at up to 200Msps .
For high energy physics application, specifically communications between the detectors and the control system can be done through power lines for configuration purposes were the data rate is not to high and depending on the segmentation of the power grid it can even be used for transferring data from the detectors.
The test card being built, also propose to test this concept using real pixel detectors. The power lines will be used to program the pixel chips registers.
In this kind of application, interference is always a problem and there are two ways to mitigate this problem. The first way is to shield the power lines and the second way is to use low frequency carrier.
There will be two different techniques concepts tested on this system. The first concept is based on On-Off Key (OOK) modulation. Here, basically the transmitter ads a carrier to the power line, the presence of the carrier or its absence will determine the zeros and ones of the communication. A representation of 1 bit is determined by timing, also there are start and stop bits marking the beginning and the end of the data The representation of this kind of modulation is presented in Fig. 6.
The representation of one bit is done in OOK where the volume represents the constrains where the signal can presented itself and be understood as one bit. In this constrains we have Pth that is the minimum power were a signal is considered valid, we also have fL and fH that is the frequency interval where the system will be accepting valid data, anything out of this window is considered noise. Finally we have tL and th that is the time interval where the signal is registered as a single bit.

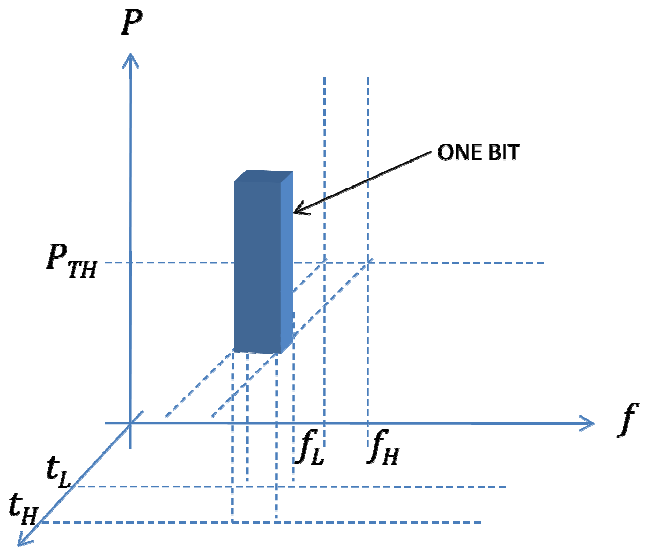


**Fig. 6 The OOK modulation space.**

One of the objectives of this board is to determine good values for this parameters. Bellow is an illustration showing a simulation of this kind of transmission in a pulsed power system.

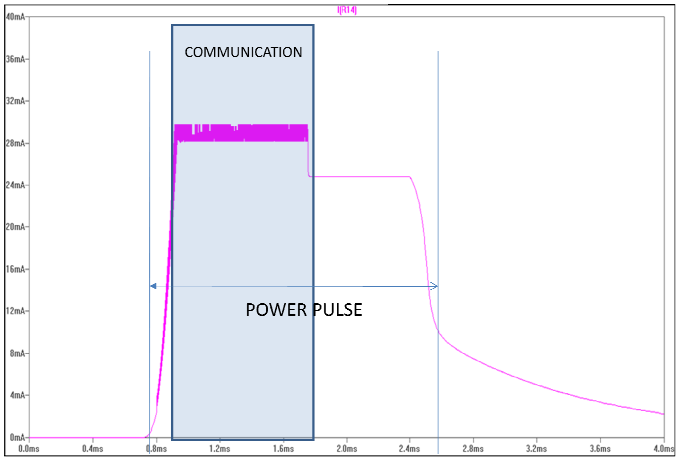


**Fig. 7 OOK over serial power.**

Notice that in the case of the ILC this communication does not need to happen necessarily while you have power, but instead it can happen in between pulses, if a pulsed system is being used.
The second technique to be tested in this board is more complex and it uses frequency shift keying (FSK) modulation, more precisely 2-FSK. This means that two discrete frequencies are used to transmit the zeros and ones. The 2-FSK used in this board uses a quadrature modulator.

## V. Conclusions

In the current stage of this project simulations had provided important feedback for the construction of a test board capable of providing a platform to reliable compare the relative

performance between the different powering options. Also, the simulation results provided encouraging results referent to data communications through the power line, specially for sending configurations signals to the modules.

Currently the board being design is in its final design phase and is expect to soon go in production.

The tests with the board will provide very important information regarding noise on the system and maximum communications speed as well as to complement the simulations with more precise data on power efficiency.

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