SLAC-TN-71-14
D. Porat/D. Ouimette
June 1971

8-BIT ADC WITH LINEAR GATE FOR CHARGE AND SUB-NANOSECOND TIME MEASUREMENTS

PART 2

USER'S GUIDE

SUPPLEMENTARY DATA TO TN-71-13

7. INTRODUCTORY NOTE

Part 1 of the ADC description, published in TN-71-13, contains the following sections:

1. Introduction, 2. Specifications, 3. Circuit Description, 4. Performance,
5. Summary of Essential Differences between the 7-bit and the 8-bit ADC's.,
6. Additional Information.

The present note discusses alignment and calibration, and contains information that may be of use in repair and for systems utilization. Numbering of sections and figures is a continuation from TN-71-13.

8. POWER REQUIREMENTS AND VOLTAGES MEASURED AT SELECTED POINTS

Table 2 shows current requirement at the standard CAMAC voltage levels used.

Table 2. Power Requirements

Voltage	Each ADC	CONTROL Module
+24 V	114 mA	O
-24 V	115 mA	O
+6 V	245 mA	110 mA
-6 V	56 mA	18 mA

Table 3 lists potentials at selected points of the ADC in its quiescent state.

Table 4 lists potentials at selected points of the CONTROL module in its quiescent state.

9. USE OF ADC IN SYSTEMS

A standard CAMAC bin can hold the following:

(i) Ten ADC's, CAMAC size-2 each. These should be located in positions 2, 4....20. Data from these modules will appear on the CAMAC bus line in response to the appropriate N-signal generated in position 24 (see iv, below).

(ii) One ADC CONTROL module, CAMAC size-1. This supplies CLOCK and CONTROL signals to all ten ADC's via the CAMAC bus. It also acts as a fan-in for DATA and has an auxiliary connector (P2) to transmit the DATA to the bin-controller. It shall be located in position 21 or 22 of the CAMAC bin.

(iii) One digital FAN-OUT, e.g., SLAC 114-123, CAMAC size-1. This module provides a standard NIM input for the CONTROL module and ten NIM signals, one for each GATE input terminal of the 10 ADC'S. It shall be located in the CAMAC bin position 21 or 22.

(iv) A CAMAC bin-controller, size-2. The details of this module depend on the system configuration. The circuit must generate the 10 N-lines required to address respective ADC's. A short cable connector on an auxiliary plug, P2, shall be provided between the bin - and the ADC-controllers to bring the DATA to convenient external bussing lines. Connector P2 also brings the external CLEAR signal from the bin - controller to the CAMAC bus. Bin - controller, when used, must be located in position 24 of the CAMAC bin.

10. ALIGNMENT PROCEDURES (Location of Adjustments is Shown in the Photo, Fig. 15)

10.1 Voltage Regulators, Fig. 12

The +20 V and -20 V regulators stabilize the voltages across the linear gate ensuring good gate-pedestal stability. They are also used to power the amplifier-integrator.

For adjustment, monitor emitters of Q26 (+20 V) or Q27 (-20 V) and adjust R105 or R110, respectively.

10.2 Gate Pedestal, Fig. 2

Apply standard NIM pulse to GATE input; no signal into DATA input. Using a scope with horizontal sweep = 2μsec/div, vertical deflection = 5 mV/div monitor output at PHA terminal. Adjust pedestal control R8 of Fig. 2 to null.

10.3 Comparator Fig. 5

Adjustment of gate pedestal must precede comparator reference voltage adjustment. Apply standard NIM pulse as in section 10.2 and monitor ADC output at "SCALER" using an oscilloscope. Turn R91 CW until one pulse, 40 to 60 nsec duration, appears on the scope. Then turn R91 two revolutions CCW. Reference pin No. 5 of A3 should now read $\approx$ 96 mV.

10.4 Discharge Constant - Current Source, Fig. 4

This is the last in a series of adjustments that must be effected in the same sequence as described in this section. Adjustment of the current source Q19-Q23 determines the slope: counts vs. charge.

(i) To adjust an individual ADC apply a standard NIM signal to the GATE input. The DATA input requires a signal that is bracketed by the GATE and has an amplitude just above the onset of saturation, e.g., -1.0 volt, 13 nsec. Adjust R88, Fig. 4, to obtain $\leq 245_{10}$ counts. This safety margin of 10 counts is suggested because of the non-ideal characteristics of limiter Q12. When properly adjusted, no ambiguity will occur due to overflow of counters A8, A9.

(ii) Due to the linearity of the instrument, it is possible to adjust a complete ADC system for equal slope. To obtain this, proceed with individual ADC's as in step (i). Then establish the slope for each ADC by measuring two points in the linear region, using suitable attenuation in the DATA path. Use the ADC with the smallest slope as the reference for adjusting the complete system.

11. CAMAC CONNECTORS

CAMAC connector pin assignment for the ADC and the CONTROL module is shown in Figs. 13 and 14 respectively. Note that the CONTROL module has an auxiliary connector, P2, to carry DATA to the chassis controller, and the external CLR to the CAMAC bus.

12. WAVEFORMS AT SELECTED TEST POINTS OF ADC

TP-1 = Input to peak detector, Fig. 9a of TN-71-13.

TP-2 = Waveform at collector of Q13A during peak detection, see Fig. 17.

TP-3 = Waveform at collector of Q16 during peak detection, see Fig. 18.

SCALER = Front panel BNC connector, CLOCK output into scaler, see Fig. 19.

CAUTION

Because of the close proximity of the pins on connector P1, it is necessary to remove power to the CAMAC bin when removing or installing CAMAC module in order to prevent short circuit damage.

Table 3

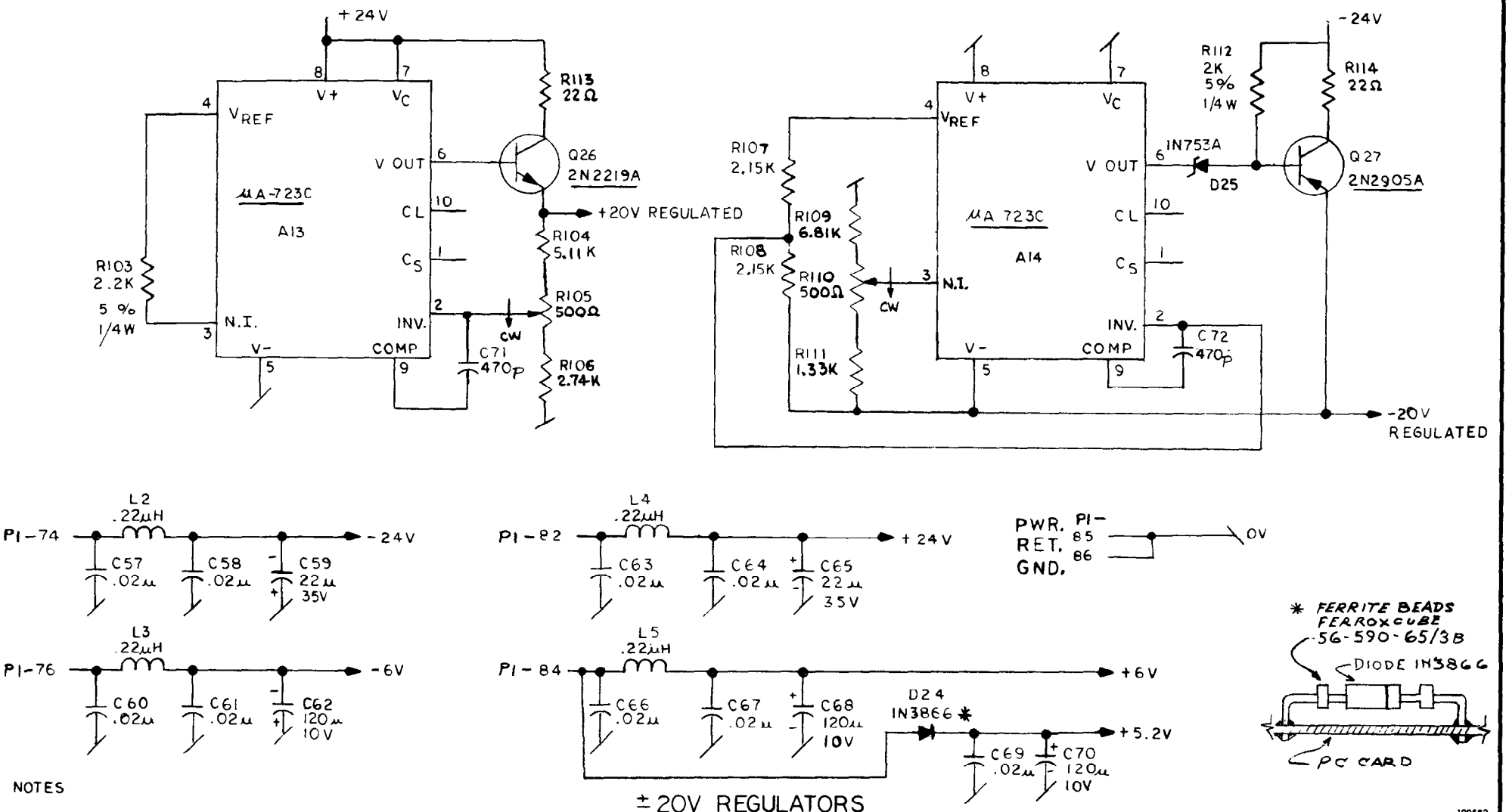
Potentials at Selected Points of the
ADC in Quiescent State

Transistor	Vc	Vb	Ve	IC	Pin No.	Volts
Q1	5.72	0.56	-0.17			
Q2	-1.05	-6.01	-6.73	A1, A2	4	-14.9 nominal
Q3	0.98	-6.38	-6.73	A1, A2	5	-14.4 nominal
Q4	6.54	0	-0.72	A1, A2	7	14.9 nominal
Q5	-0.26	6.54	7.22	A1	6	0
Q6	7.27	-0.26	-0.93	A2	6	-0.1
Q7	3.88	7.34	7.98	A3	4	-0.1
Q8	8.01	3.88	3.25		5	0.95 nominal
Q9	1.60	7.10	7.85	A7	6	3.7 nominal
Q10	6.95	-0.29	-0.93		9	4.5 nominal
Q11	-1.03	6.95	7.60	A8, A9	1	4.4 nominal
Q12	0	4.48	0	A8, A9	13	5.2 nominal
Q13A	3.88	0	-0.68	Linear	Gate at Jct	D2, D4 -0.30 V
Q13B	5.08	-0.1	-0.68	Linear	Gate at Jct	D3, D5 0.27 V
Q14	0.08	0.75	0			
Q15	5.08	12.00	12.64			
Q16	1.50	5.08	5.78			
Q17	-0.1	6.00	5.78			
Q18	-0.1	0.6	-0.15			
Q19	-0.1	-6.00	-4.69			
Q20	-0.98	-3.97	-4.69			
Q21	-4.69	-7.41	-8.02			
Q22	-7.41	-8.59	-9.22			
Q23	-8.34	-8.59	-9.22			
Q24	-1.07	-1.49	-2.33			
Q25	0	-2.56	-2.33			
Q26	22.19	20.70	20.00			
Q27	21.91	-20.73	-20.00			

Table 4

Potentials at Selected Points of
CONTROL Module in its Quiescent State

	Vc	Vb	Ve	
Q1	3.60	0	-0.77	
Q2	6.00	-0.36	-0.77	
Q3	6.00	0	0	
Q4	6.00	-0.98	0	
Q5	0.07	0.84	0	
Q6	4.63	4.15	3.49	Without Crystal
Q7	0.25	0.84	0	



NOTES

2. ALL RESISTORS ARE 1/4 W 1% UNLESS OTHERWISE SPECIFIED.

FIG. 12

8-Bit ADC. Voltage Regulators.

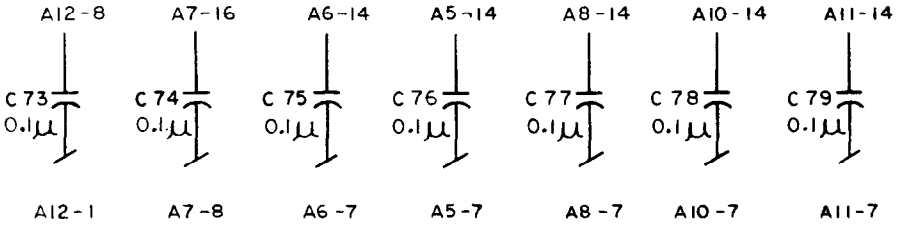
±20V REGULATORS

190582

SCALE:	DO NOT SCALE DRAWING	~~NEXT ASSEMBLY~~: SHT 5 OF 6
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. TOLERANCES: BREAK EDGES .005-.015 FRACT. ± INT. COR. .015 R. MAX. DEC. ± ANGLES ± ALL SURFS. √	STANFORD LINEAR ACCELERATOR CENTER U. S. ATOMIC ENERGY COMMISSION STANFORD UNIVERSITY STANFORD, CALIFORNIA	8 BIT ANALOG TO DIGITAL CONVERTER FOR NANOSECOND PULSES
ENGR. D. PORAT DFTS. HABER CHK. VC	APPROVALS D Porat	SD-114-121-00-R0 B

CAMAC CONNECTOR, P1, PIN ALLOCATION FOR ADC

FUNCTION	SYMBOL	CAMAC LINE	P1-PIN Nº
UNCLAMP	UC	W20	29
CLOCK	CLK	W22	27
INHIBIT	INH	W24	25
CLEAR	C	C	15
STROBE	N	STA. Nº	17
READ DATA	$\overline{2^7}$	R8	65
	$\overline{2^6}$	R7	66
	$\overline{2^5}$	R6	67
	$\overline{2^4}$	R5	68
	$\overline{2^3}$	R4	69
	$\overline{2^2}$	R3	70
	$\overline{2^1}$	R2	71
READ DATA	$\overline{2^0}$	R1	72
POWER	-24 V	-24 V	74
POWER	-6 V	-6 V	76
POWER	+24 V	+24 V	82
POWER	+6 V	+6 V	84
POWER RET	0	0 V	85
POWER RET	0	0 V	86



NOTE:
C80-C88 ARE FILTER CAPACITORS DISTRIBUTED ON POWER BUSS.

FIG. 13

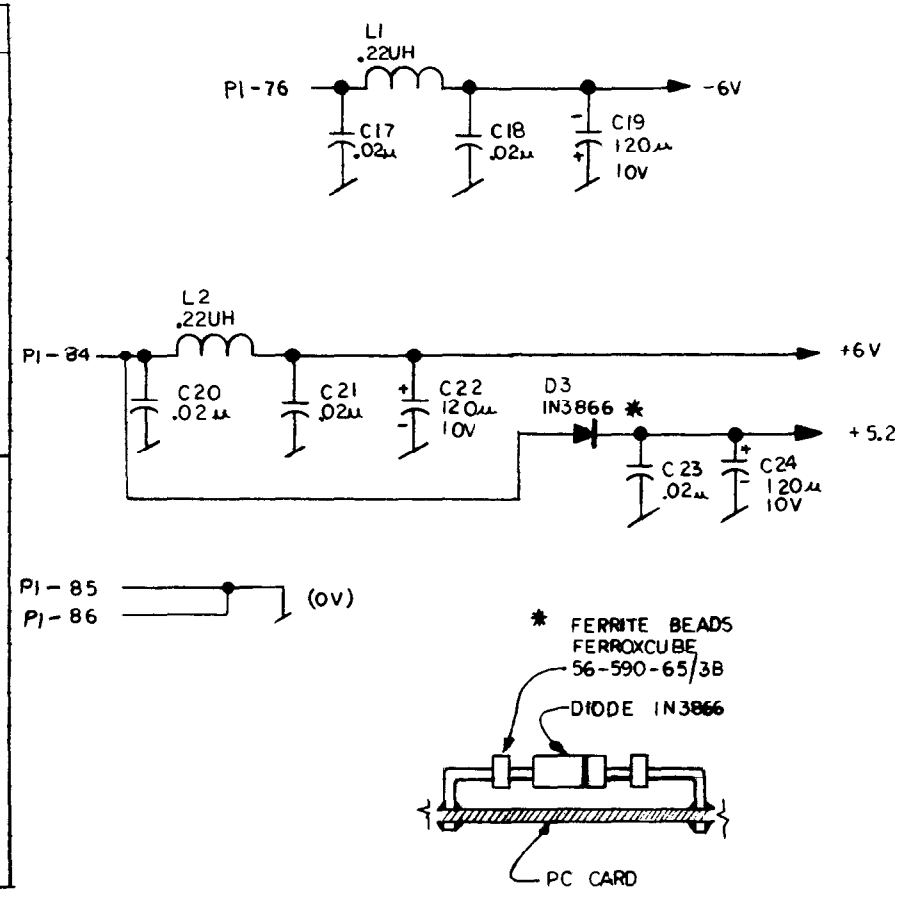
190583

CAMAC Connector, P1. Pin Allocation for ADC.

SCALE:	DO NOT SCALE DRAWING	~~NEXT ASSEMBLY~~: SHT 6 OF 6
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. TOLERANCES: BREAK EDGES .005-.015 FRACT. ± INT. COR. .015 R. MAX. DEC. ± ANGLES ± ALL SURFS. √	STANFORD LINEAR ACCELERATOR CENTER U. S. ATOMIC ENERGY COMMISSION STANFORD UNIVERSITY STANFORD, CALIFORNIA	8 BIT ANALOG TO DIGITAL CONVERTER FOR NANOSECOND PULSES
	ENGR. D. PORAT DFTS. HABER CHK. VIC G. APPROVALS L. Paros	SD-114-121-00-R0 B

CAMAC PIN ALLOCATION FOR CONTROL MODULE

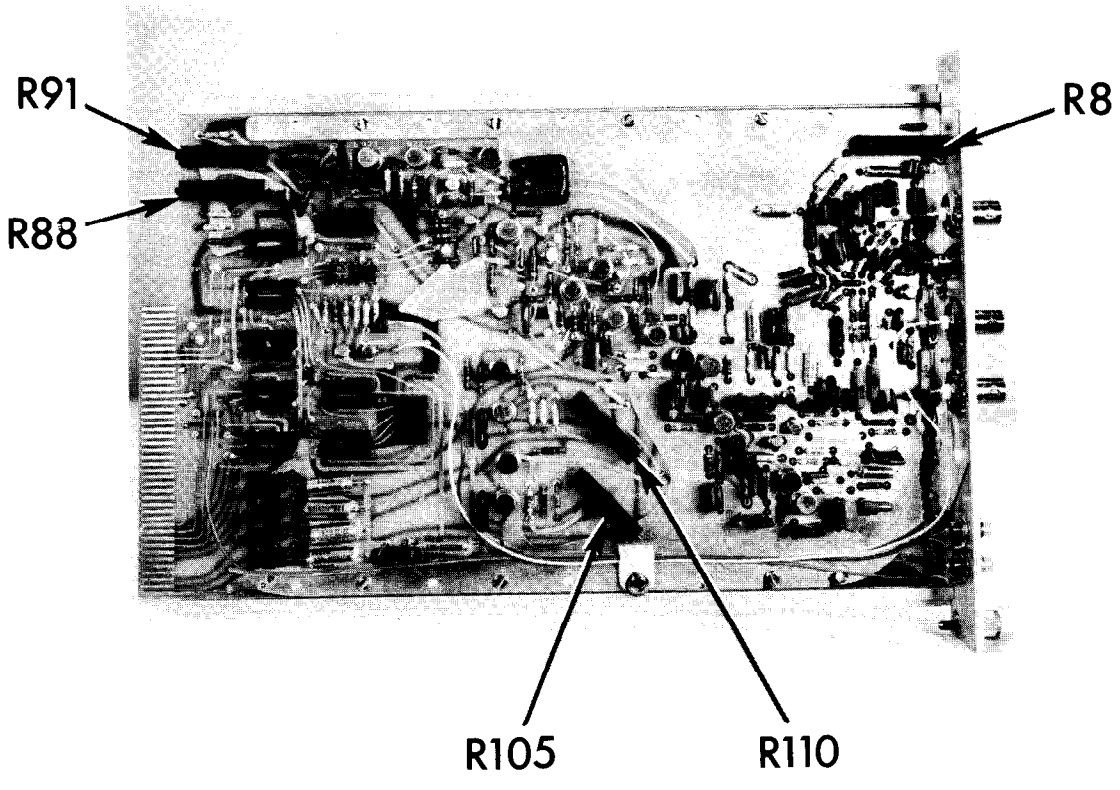
FUNCTION	SYMBOL	CAMAC LINE	PIN No.
UNCLAMP	UC	W20	P1-29
CLOCK	CLK	W22	-27
INHIBIT	INH	W24	-25
CLEAR	C	C	-15
BIT 0	2^0	R1	-72
1	2^1	R2	-71
2	2^2	R3	-70
3	2^3	R4	-69
4	2^4	R5	-68
5	2^5	R6	-67
6	2^6	R7	-66
BIT 7	2^7	R8	P1-65
BIT-0	2^0		P2-17
-1	2^1		-16
-2	2^2		-15
-3	2^3		-14
-4	2^4		-13
-5	2^5		-12
-6	2^6		-11
BIT-7	2^7		-10
CLEAR	C		P2-20
POWER	+6V	+6V	P1-84
POWER	-6V	-6V	P1-76
PWR RET	O	O	P1-85
PWR RET	O	O	P1-86



NOTE:
C25-C32 ARE FILTER CAPACITORS DISTRIBUTED ON POWER BUSS.

FIG. 14 CONTROL Module. CAMAC Connector P1 and Auxiliary Connector, P2. Pin Allocation. 190584

SCALE:	DO NOT SCALE DRAWING	NEXT ASSEMBLY: SHT. 3 OF 3
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. TOLERANCES: BREAK EDGES .005-.015 FRACT. ± INT. COR. .015 R. MAX. DEC. ± ANGLES ± ALL SURFS. √	STANFORD LINEAR ACCELERATOR CENTER U. S. ATOMIC ENERGY COMMISSION STANFORD UNIVERSITY STANFORD, CALIFORNIA	8 BIT ANALOG TO DIGITAL CONVERTER CONTROL MODULE
	ENGR. D. PORAT DFTS. DONALD HUDSON CHK.	APPROVALS
		SD-114-122-00-R0 B



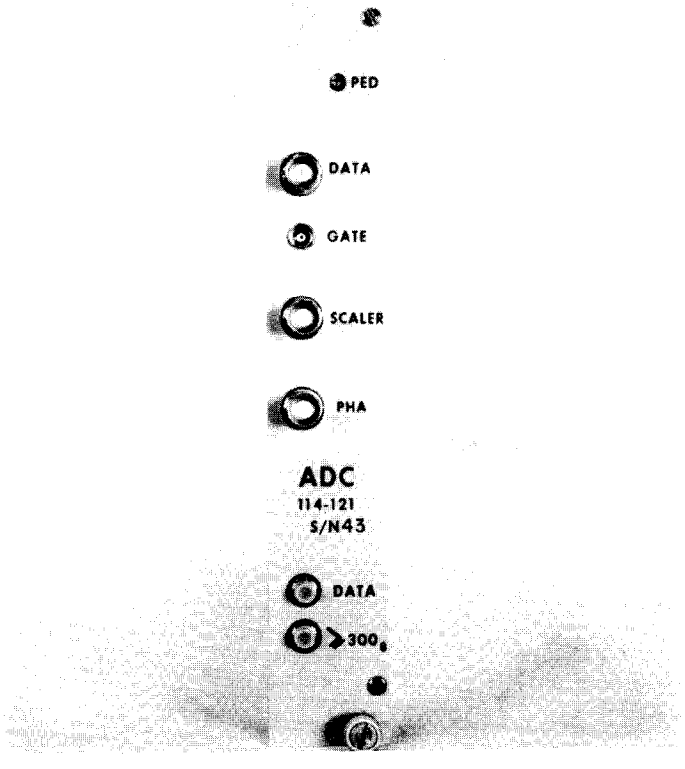
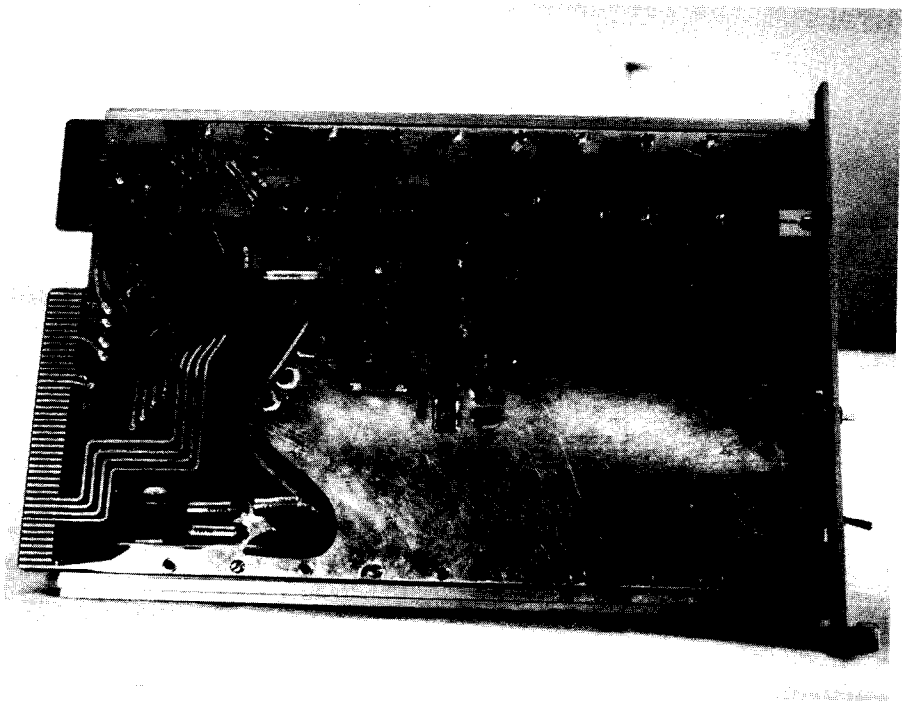


Fig. 15 8-Bit ADC with Location of Adjustments Shown.



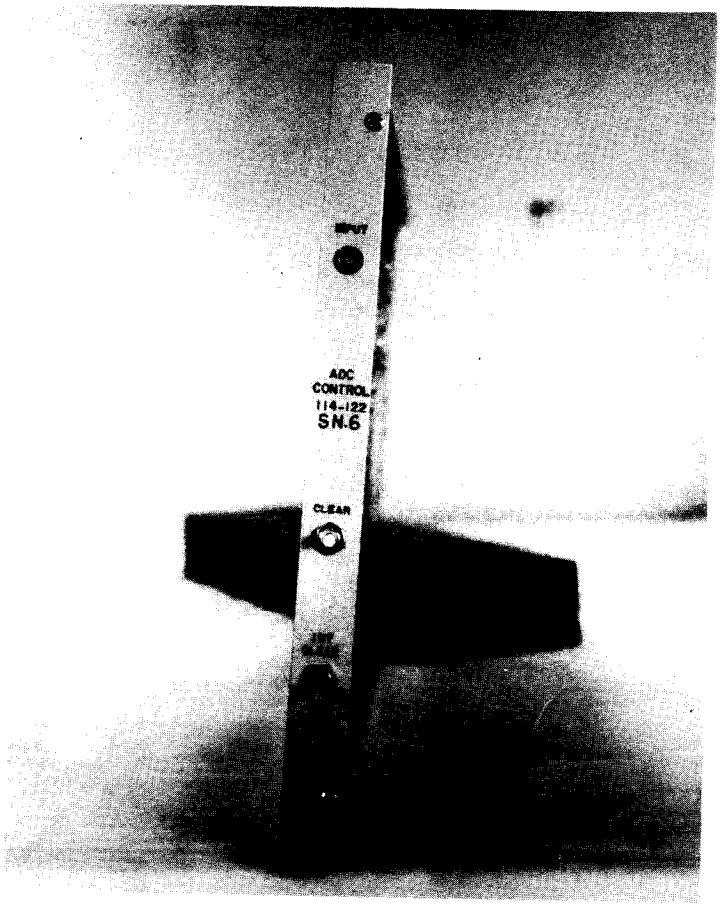
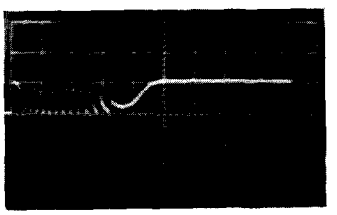


Fig. 16 CONTROL Module.

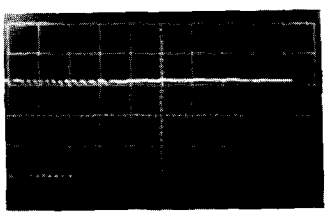
1905A6



1 μsec/div.
2 V/div.

Fig. 17

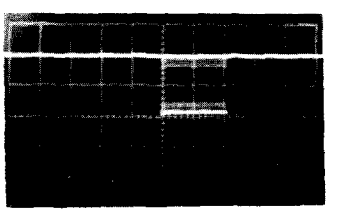
Waveform at TP2, Collector of Q13A during Peak Detection.
Hor.: 1 μsec/div. Vert.: 2 V/div.



1 μsec/div.
0.5 V/div.

Fig. 18

Waveform at TP3, Collector of Q16 During Peak Detection.
Hor.: 1 μsec/div. Vert.: 0.5 V/div



5 μsec/div.
0.2 V/div.

Fig. 19

1905A1

Output at SCALER Terminal (BNC). Data Signal Applied at t=0.
Hor.: 5 μsec/div. Vert.: 0.2 V/div.