

Electronics and triggering challenges for the CMS High Granularity Calorimeter

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Electronics and triggering challenges for the CMS High Granularity Calorimeter

A. Lobanov on behalf of the CMS collaboration

*Laboratoire Leprince-Ringuet — École polytechnique, IN2P3/CNRS
91128 Palaiseau, France*

E-mail: artur.lobanov@llr.in2p3.fr

ABSTRACT: The High Granularity Calorimeter (HGCAL), presently being designed by the CMS collaboration to replace the CMS endcap calorimeters for the High Luminosity phase of LHC, will feature six million channels distributed over 52 longitudinal layers. The requirements for the front-end electronics are extremely challenging, including high dynamic range (0.2 fC–10 pC), low noise ($\sim 2000 e^-$ to be able to calibrate on single minimum ionising particles throughout the detector lifetime) and low power consumption (~ 20 mW/channel), as well as the need to select and transmit trigger information with a high granularity. Exploiting the intrinsic precision-timing capabilities of silicon sensors also requires careful design of the front-end electronics as well as the whole system, particularly clock distribution. The harsh radiation environment and requirement to keep the whole detector as dense as possible will require novel solutions to the on-detector electronics layout. Processing the data from the HGCAL imposes equally large challenges on the off-detector electronics, both for the hardware and incorporated algorithms. We present an overview of the complete electronics architecture, as well as the performance of prototype components and algorithms.

KEYWORDS: Calorimeters; Front-end electronics for detector readout; Trigger concepts and systems (hardware and software)

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1 The CMS HGICAL project

The Large Hadron Collider (LHC) is currently the largest and most powerful collider worldwide. Despite the excellent physics results already obtained at the LHC, an increase of the integrated luminosity by an order of magnitude will help measure important Standard Model parameters with higher precision and possibly uncover new phenomena. Therefore, an upgrade of the accelerator complex called High Luminosity LHC (HL-LHC) is foreseen in the years 2024–2026 and will allow for a three to four times higher instantaneous luminosity with respect to the current LHC operation, providing 3000 fb^{-1} of integrated luminosity within 10 years.

The increased intensity will also result in higher particle fluxes, radiation levels and simultaneous interactions (pileup) occurring at the LHC experiments. In order to cope with the more challenging environment and mitigate effects of radiation damage, the CMS collaboration [1] is planning an upgrade of its detector systems and infrastructure.

Among these upgrades is the replacement of the current calorimeter endcaps, which will not survive the radiation levels anticipated at the HL-LHC, with a high granularity calorimeter (HGICAL) [2, 3] comprising a total of 52 longitudinal layers of finely segmented silicon sensors and scintillators (figure 1). Silicon is placed in areas of higher particle flux and radiation, whereas scintillators are used in lower radiation areas. In many aspects this project profits from previous developments within the CALICE Collaboration for the SiW-ECAL [4] and AHCAL [5].

The HGICAL silicon part is tiled with hexagonal sensors of different active thickness (120, 200 or $300 \mu\text{m}$, see figure 1, right). The cell size also differs (0.5 cm^2 for the thinnest ones, 1 cm^2 for the others), resulting in 192 to 432 channels per 8" sensor respectively. In order to reduce the radiation damage of the silicon sensors, the full endcaps are cooled down to -30°C , and the thinner and more granular wafers are placed at higher pseudorapidity regions. The scintillator part comprises single tiles of constant azimuthal angle decreasing in size with increasing pseudorapidity from 32 cm^2 to 4 cm^2 . The readout of each individual scintillator tile is performed with silicon photomultipliers (SiPMs). A total of 6 million silicon cells and 400 000 scintillator tiles covers an area of ~ 600 and $\sim 500 \text{ m}^2$, respectively. Single silicon wafers and arrays of scintillator tiles are assembled into individual modules (see section 2), of which there are a total of 27000 and 4000, respectively.

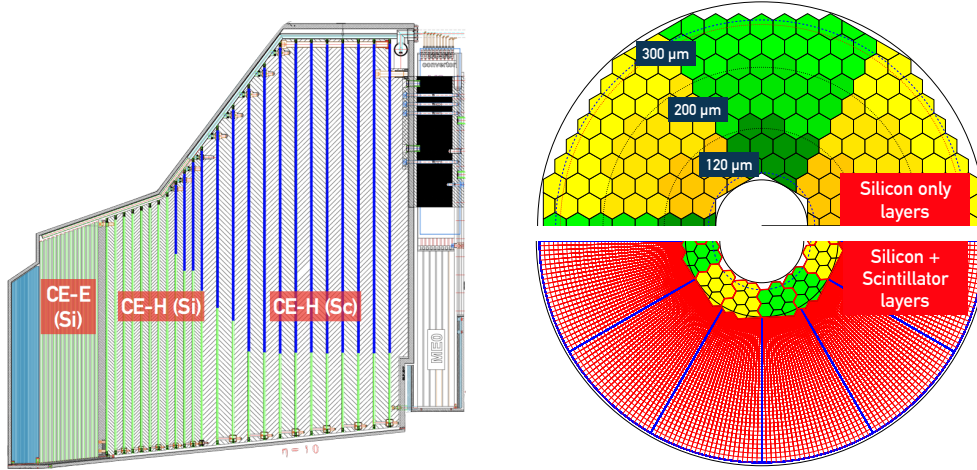


Figure 1. Schematic illustration of an HGCAL endcap highlighting the silicon and scintillator compartments in green and blue, respectively (left). Layout of a silicon-only (top) and mixed silicon-scintillator (bottom, not to scale) layer indicating the different silicon wafer thickness regions (right).

Electronics and trigger challenges The high granularity of the HGCAL and environment of the HL-LHC pose a big challenge for the detector design, in many aspects exceeding the demands to the electronics and trigger requirements of the current LHC detector.

In the anticipated HL-LHC running scenario with on average 200 pileup interactions the cell occupancy in some HGCAL areas may reach up to 60%, whereas the current Run-2 pileup level is four times lower. This high flux of particles directly translates into large radiation doses, therefore, requiring the electronics to be radiation hard up to 2 MGy. The readout electronics needs to be sensitive to large signals of the order of 3000-5000 minimum ionizing particles (MIP), which occur in TeV particle showers, but as well to single MIP deposits in order to calibrate the individual channels.

The current CMS calorimeters feature about 200 thousand channels in total, whereas the HGCAL will need to power, control and read out about 6 million channels. This sets stringent requirements on the electronics power consumption. A total power consumption of 110 kW is expected per each endcap. The data traffic will also increase with trigger rates above 750 kHz. Finally, it is intended to reuse and incorporate as many common parts as possible from the current HL-LHC developments, such as the low-power gigabit transceiver (lpGBT) and versatile link data transfer system.

Figure 2 (left) shows a general overview of the on- and off-detector electronics architecture. The sensors are read out by very front-end (FE) readout ASICs. Digitized trigger data are sent at 40 MHz to concentrator ASICs, where the data are selected, reformatted and re-transmitted to the back-end (BE) trigger electronics off the detector. DAQ data are stored in buffers with a latency of 12.5 μ s and transferred to the DAQ BE electronics after the L1 trigger accept.

2 Front-end electronics

In order to ensure the best compactness of the detector, the sensitive layers have to be as thin as possible, while hosting the full set of detector front-end electronics, power distribution and

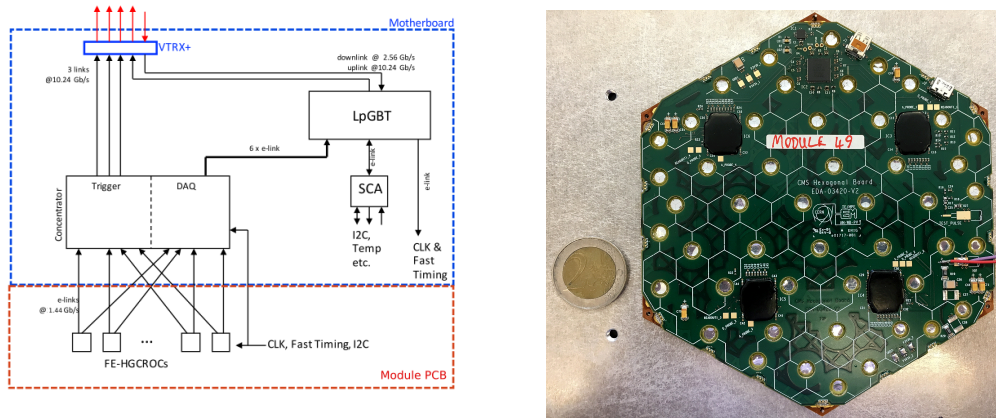


Figure 2. General architecture of the HGCAL on- and off-detector electronics (left). Front-end ASICs are mounted on a module PCB, glued to the sensor. Concentrator and control ASICs are mounted on a motherboard, located a few mm above the module PCB. Photo of a 6" silicon module prototype for beam tests (right).

communication. Due to the more demanding requirements, we focus in this paper on the silicon part of the calorimeter.

The hexagonal silicon detector modules comprise multiple layers with a total thickness below 6 mm. In addition to the sensor there are 2 printed circuit boards (PCB): the first (called hexaboard) hosts the very-FE readout ASICs connected to the silicon sensor with wire-bonds through holes; the second PCB (called motherboard) serves several hexaboards to provide connectivity, power, data concentration, trigger data generation and bi-directional communication through the concentrator using lpGBT links. Design studies for both boards are currently ongoing and figure 2 (right) shows a 6" module developed for beam tests in 2017 [7].

Readout ASICs The FE readout ASIC sits at the heart of the detector and is subject to critical requirements that drive the performance of the detector. For HGCAL, a system-on-chip design was chosen featuring analog charge and time measurement, digitization, data and trigger processing. A common ASIC for both the silicon and scintillator parts is envisaged, which need to satisfy a low power consumption of < 20 mW/channel, low noise of $< 2000 e^-$, be tolerant to single event effects and provide high-speed data and trigger links above 1.2 Gb/s.

In order to be able to perform data-driven calibration throughout the detector lifetime, the ASIC will need to be sensitive to signals deposited by single MIPs. The largest expected signals in high-energy showers are of the order of 3000 MIP. Therefore, the ASIC will need a high dynamic range of 0.2–10000 fC. This range can be ensured with a good resolution by combining a traditional charge sampling from a shaper output in the range of 0.2–100 fC using an 11-bit ADC and a Time-over-Threshold (TOT) scheme covering the 0.1–10 pC range with a 12-bit TDC.

A precise timing information will help to discriminate showers from pileup. Such a measurement is performed by a Time-of-Arrival (TOA) circuit in the ASIC with a 10-bit TDC. The single-channel resolution is required to be at the level of 40 ps for signals above 50 fC, resulting in a 20 ps resolution for clusters consisting of multiple cells.

The development of the HGCAL readout chip (HGCROC) is following several steps of design and validation, with the final submission being scheduled for mid 2020.

SKIROC2cms Initial beam tests of the HGCAL design were performed with the SKIROC2 [6] developed for the CALICE SiW-ECAL. This ASIC is implemented in SiGe 350 nm technology and features 64 channels with single low and high gain charge samples per event. Based on this chip, the SKIROC2cms [8] was designed for beam tests and adapted to CMS-like running conditions with a 40 MHz clock and sampling, including blocks for the evaluation of the TOT and TOA mechanisms. The modified ASIC was submitted and received in the first quarter of 2016.

Like the SKIROC2 chip, the SKIROC2cms samples and digitizes the charge with a high and low gain, but also includes an analog memory for eleven consecutive clock cycles. The corresponding slow shaping time was chosen to be 40 ns for lower noise. The TOA is fed through a fast shaper with 5 ns shaping time, while the TOT is directly coupled to the preamplifier. The TDC for the TOA and TOT blocks have a ~ 20 ps binning and 50 ps jitter.

Extensive tests of the SKIROC2 cms have been performed on single-ASIC test boards as well as mounted on the hexaboard and silicon detector modules. Figure 3 (left) shows the charge response characteristics for the low & high gains and TOT of a single chip channel on a hexaboard. Temperature tests showed acceptable variations of the signal responses for these measurements. In addition, the TOA transfer characteristics, trigger efficiency, jitter and time-walk were studied and found to be within the design characteristics [9].

Test vehicles A set of two test vehicles (TV) was developed in the period of 2016–2017 in order to validate and measure some first building blocks of the HGCROC in a commercial 130 nm CMOS technology [10]. The TV1 was targeted towards the investigation of various CR-RC shapers and different circuits for the TOT discriminators and the study of noise induced by digital activity. Different options for shapers and ADC, such as an 11-bit SAR-ADC, were studied in the TV2. A first implementation of a 32×512 RAM designed at CERN was successfully tested.

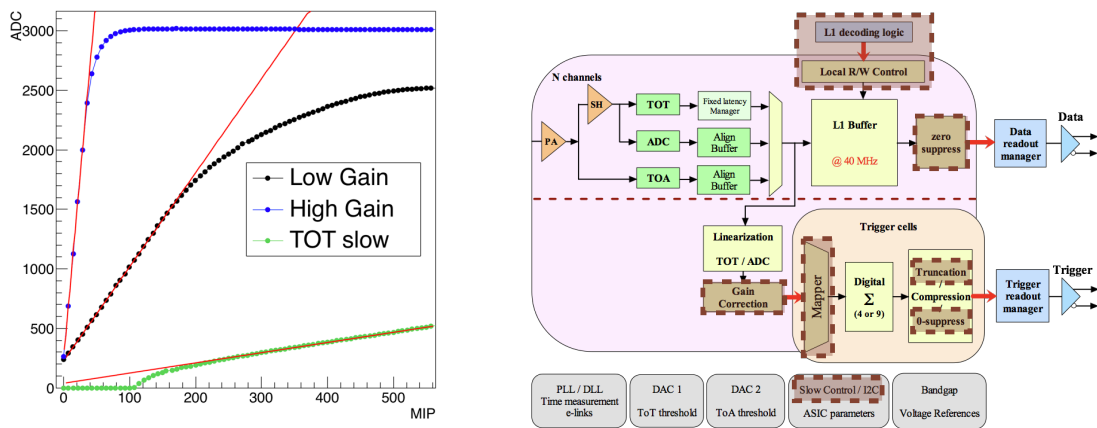


Figure 3. Transfer characteristics for the low/high gain and TOT of the SKIROC2cms (left). Block diagram of the HGCROCv1 (right). The brown boxes indicate blocks not yet included in this version of the ASIC.

HGCROC A first version of the final ASIC HGCROCv1 was submitted mid 2017 and is expected to become available for tests towards the end of the year. The number of channels of this ASIC was reduced to 32 instead of the anticipated 72 for development and cost reasons. The chip features most of the analogue and mixed analogue-digital blocks, while some of the missing digital parts are foreseen to be incorporated in the next version.

The HGCROCv1 includes a TOA circuit and two variants of TOT circuits. The 11-bit SAR-ADC operates at 40 MHz and the data are read out at 320 MHz. A shift register with triple voting similar to the SKIROC2cms is implemented for the slow control configuration. The simplified trigger part is discussed in section 3.

A first full version of the chip (HGCROC-DV1) is expected to be submitted by mid 2018, with the next iteration following in 2019. The production run of the final ASIC is foreseen for mid 2020.

3 Trigger primitive generation

As mentioned in section 1, the upgraded L1 Trigger will operate at rates exceeding 750 kHz. Given the high number of readout channels and large data size, a raw data flow of about 8 Pbit/s is generated. Since this amount of data is incompatible with cost and link placement, a drastic data reduction has to be performed from the detector front-end to the back-end. The maximum allowed trigger latency is $12.5 \mu\text{s}$.

The trigger primitive (TP) generation starts in the HGCROC with the linearization of the ADC and TOT signals for each channel. A combination of channels into trigger cells (TC) according to their geometrical alignment (figure 4, left) allows for a further reduction of the data size. Each sensor comprises 48 TCs. The concentrator ASIC on the motherboard selects a fraction of these TCs depending either on an individual threshold or selecting a fixed number of the highest energy TCs. The selection algorithms are currently being evaluated in order to provide the best data reduction with the least impact on physics performance.

At this stage, a data rate of 40 Tbit/s per second is expected, which is carried off each endcap by ~ 4000 optical links. Figure 4 (right) shows the concept of the two-stage trigger primitive generation in the detector back-end. The first stage comprises one board per trigger layer, allowing

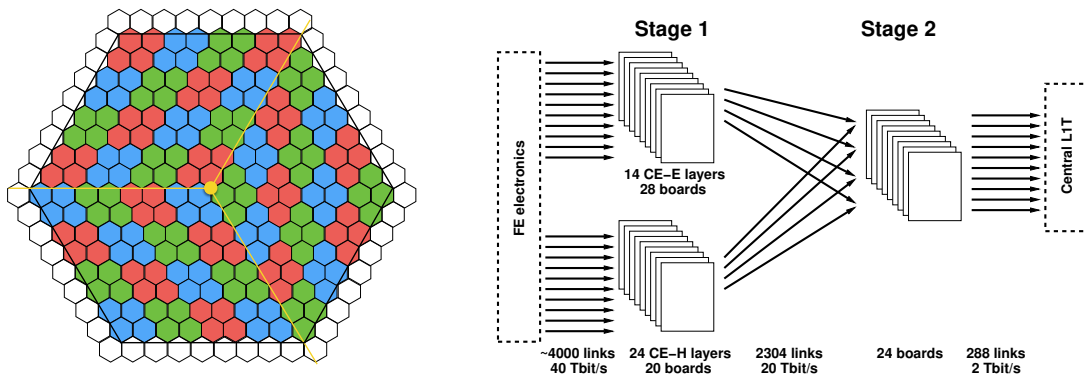


Figure 4. Layout of 2×2 trigger cells in a 200 or 300 μm thick Si sensor (left). Stages of the back-end trigger primitive generator (right).

for a dynamical 2D clustering of the trigger cells. Next, the 2D clusters are fed into a time multiplexed second stage, where each of the 24 boards forms 3D clusters corresponding to a single bunch crossing. At the TP generator exit the data rate is reduced to 2 Tbit/s and supplied to the central CMS L1 Trigger, where the HGCAL clusters are combined with reconstructed tracks from the CMS track trigger.

Both the data acquisition (DAQ) and TP generator systems require boards with high I/O and significant processing power. It is planned to use generic boards developed for the whole CMS trigger and DAQ systems, and not only HGCAL. Current development of boards in the ATCA format shows the possibility of providing almost 100 I/O links rated to about 16 Gbit/s. This processing can be performed by Kintex or Virtex Ultrascale FPGAs. First firmware simulations of the stage 1 algorithms show perfect agreement with software simulations. The 2D algorithm has been efficiently tested on a Virtex 7 FPGA and the latency is estimated to be up to 1 μ s.

4 Outlook & summary

The CMS High Granularity Calorimeter is a very challenging detector project for the HL-LHC upgrade. The harsh radiation environment, high pile-up and stringent requirements on the performance together with the tight schedule present a high demand on the detector electronics development.

A variety of front-end readout ASICs has been and will be investigated in order to meet the requirements of the HGCROC. Extensive use has been made from previous developments for the CALICE collaboration, such as the SKIROC2 ASIC and its derivative SKIROC2cms. A first version of the HGCROC is currently being evaluated, while the complete ASIC implementations will be submitted and validated in 2018-2019. The final submission of the HGCROC is anticipated by mid 2020.

The trigger chain is being developed within the HGCROC as well as in the following concentrator ASIC and back-end trigger primitive generator. This multi-stage approach allows for a sufficient data reduction while preserving the advantage of the fine 3D granularity of the HGCAL. The specifications of the BE system are to be fixed by mid 2020.

Acknowledgments

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