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HIGH PERFORMANCE GENERIC BEAM DIAGNOSTIC SIGNAL PROCESSOR FOR SHINE*

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Abstract

A generic signal processor has been developed for beam diagnostic system in SHINE. The stand-alone processor is used for the signal processing of stripline BPM, cavity BPM, cold button BPM, beam arrival measurement, bunch length measurement and other diagnostic systems. The main core is a SoC FPGA, which contains both quad-core ARM and FPGA on a chip. The ARM runs LINUX OS and EPICS IOC, and FPGA performs peripheral interfaces and high-speed real-time signal processing. An FMC carrier ADC board is mounted, which can sample 4 channels input signal with a maxi-mum sampling rate of 1 GSPS. The processor is equipped with a White Rabbit timing card, which can realize 1 MHz high repetition rate synchronous measurement. Lab test results and on-line beam tests prove that the processor has high performance. This paper will introduce the processor development and applications on SHINE.

INTRODUCTION

The Shanghai HIgh repetitioN rate XFEL and Extreme light facility (SHINE) is 30 m underground, with a total length of 3.1 km in Shanghai. The SHINE was constructed adjacent to the Shanghai Synchrotron Radiation Facility (SSRF) and the Shanghai Soft X-ray Free Electron Laser (SXFEL). It is initiated at the end of 2018, and to be completed at 2027. The facility is composed by injector, superconducting LINAC, undulators and beamlines. To meet different data acquisition requirements, we have developed a general beam diagnostics signal processor, which is used for the signal processing of stripline BPM, cold BPM, cavity BPM, BAM and BLM. SHINE needs about 500 beam diagnostics processors.

Other facilities have also developed generic electronics, such as European-XFEL [1] and SLAC LCLS-II [2]. Due to limitations in electronic device performance, a multi-FPGA system of EXFEL was developed, based on the VME64x architecture. The ADCs include a 16-bit, 160 MHz sampling rate ADC and a 12-bit, 500 MHz sampling rate ADC for different applications. The LCLS-II is based on the ATCA architecture and uses Kintex series FPGAs. The ADCs are16-bit with a sampling rate of 370 MHz to meet various application requirements.

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We have developed the self-developed Digital Beam Position Measurement processor (DBPM) [3], which was the first employed in the Dalian Coherent Light Source (DCLS) and the SXFEL. The DBPM is a one stand-alone processor with FPGA carrier board, an ADC board, and an ARM board. The ADC board has four input channels, the maximum sampling rate is 125 MHz, resolution is 16 bits, and bandwidth is 650 MHz. A XILINX Virtex5 FPGA is used as the core component on the carrier board.

The maximum repetition rate is 50 Hz of SXFEL. To meet the requirements for a 1 MHz high repetition rate and synchronized data acquisition and processing for SHINE, we developed the Generic Beam Diagnostic Signal Processor.

HARDWARE DESIGN

The processor is designed as a 1 U height standalone device, as Fig. 1. From the Fig. 2, we can see the core component is a Xilinx ZCU15EG FPGA, an ADC daughter board connected through FMC HPC interface, and a White Rabbit timing daughter board connected through FMC LPC interface. The external logic interfaces include 8 GB DDR4 on the PL (Programmable Logic) side and 4 GB DDR4 on the PS (Processing System) side to store raw ADC waveforms and processed data, two RJ45 connectors for Ethernet communication, 10Gbps SFP+ port, JTAG, SD slot, *et al.*. Table 1 lists the specification of processor.

Figure 1: Generic processor.

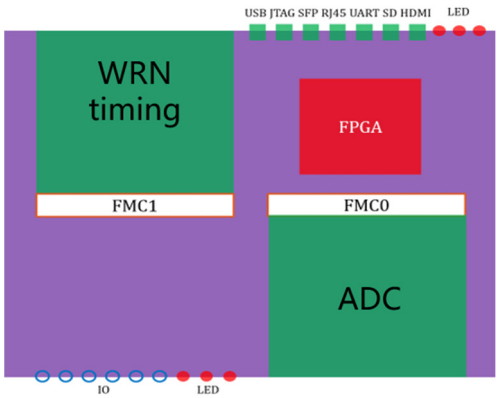

Figure 2: Processor structure.

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The ADC board has four input channels, resolution is 14 bits, the maximum sampling rate of 1 GSPS, and a 2 GHz bandwidth. It utilizes the JESD204B high-speed serial interface to enable high-bandwidth data transmission with the FPGA. ADC sampling daughter board support a 216.6 MHz external clock and a local clock, as input sampling clocks for phase-locked loop (PLL). The PLL generates the final output sampling clock, which is used by the ADC.

The White Rabbit timing board provides the bunch id and trigger signals, and it enables synchronized data acquisition for all electronics.

Table 1: Processor Specifications

Parameter	Value
Channels	4
Bandwidth	2 GHz
ADC bits	14
Max ADC rate	1GSPS
FPGA	Xilinx ZCU15EG
Clock	External
Trigger	Ext./Self/Period
SFP	2 UDP, 2 Aurora
User GPIO	12
LED	8
Interlock	Lemo
PL DDR4	2 GB
GPIO	12
Software	Linux/EPICS

SOFTWARE DESIGN

The system uses the Debian operating system and EPICS bases 7.0.7, as Fig. 3. It integrates the Asyn support package and ProcServ to manage and operate the IOC, enabling automatic startup, remote access, and Chrony time synchronization. The EPICS Autosave tool is utilized to automatically save the IOC's status and recorded values, and to restore the saved state after a system restart. The SHINE IOC is used to monitor ADC waveforms, beam position, bunch ID, and interlock signals. EPICS PyDM, a Python-based toolkit, is employed to create the GUI, allowing users to monitor PVs in the EPICS system and display information on LCD screens. Fig. 4 is the block diagram of generic processor.

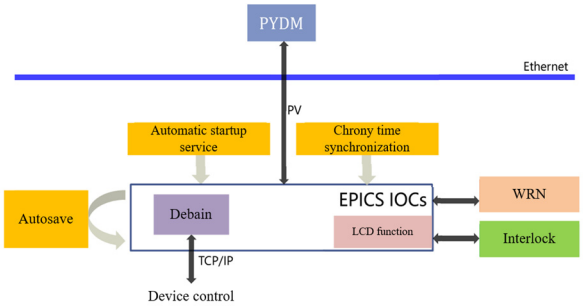

Figure 3: Processor software function block diagram.

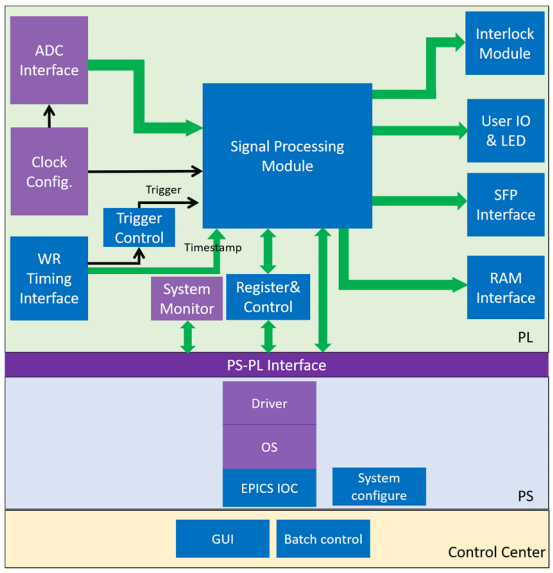

Figure 4: Block diagram of generic processor.

APPLICATION ON SHINE AND PERFORMANCE EVALUATION

Firstly, we conducted performance testing of the processor in the laboratory. ENOB (Effective Number of Bits) measured by using RF signal sources of 50 MHz and 500 MHz are respectively 10.8 bits and 10.3 bits. Furthermore, the relative position error measured using the Δ/Σ method with the stripline BPM was 5.2×10^{-5} shown in Fig. 5 (left), while the relative amplitude error measured using the x/r method with the cavity BPM was 1.0×10^{-4} shown in Fig. 5 (right). Both measurements significantly outperformed the standard threshold of 1.0×10^{-3}.

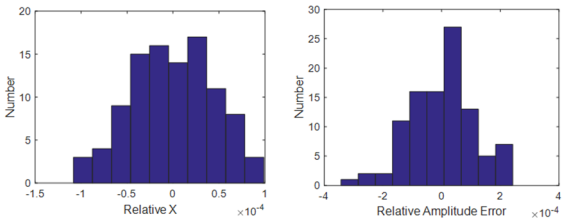

Figure 5: The relative position error of stripline BPM (left) and the amplitude position error of cavity BPM (right).

Figure 6: Photo of processor cabinet.

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In October 2023, the processors were deployed in the injector section of SHINE, as shown in Fig. 6. Beam commissioning was carried out, marking the first verification of the 1 MHz high repetition rate and enabling charge measurements, as illustrated in Fig. 7.

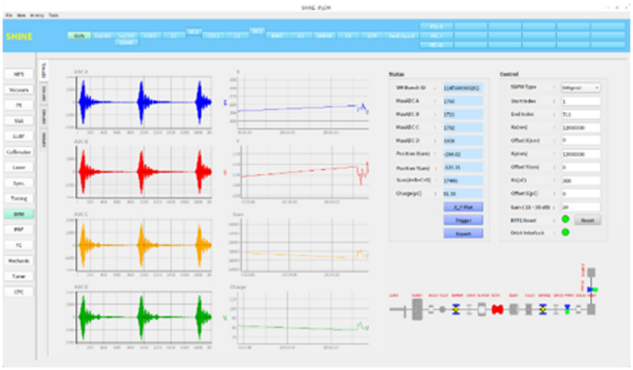

Figure 7: SHINE Signal Processor PYDM Main Interface.

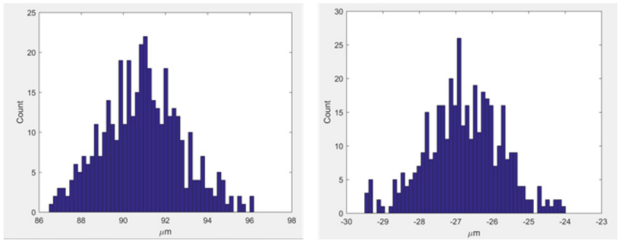

Figure 8: Resolution comparison between the RF front-end module combined with the processor (left) and the processor alone (right).

Figure 7 is the SHINE Signal Processor PYDM Main Interface, which shows SHINE has realized 1MHz high repetition rate synchronous measurement.

On-line beam tests at SHINE injector shows resolution of Stripline BPM electronics is 1.8 μm for the combined RF front-end module and processor, shown as Fig. 8 (left), with a relative error of 1.6×10^{-4}. And the resolution of processor alone is 1.0 μm, shown as Fig. 8 (right), with a relative error of just 8.2×10^{-5}.

CONCLUSION

We have completed the installation of the processors in the injector section and achieved their application. During beam commissioning, we have measured the first beam in SHINE and confirming a high repetition rate of 1 MHz. To date, 270 units have been delivered. This lays the groundwork for the next step in beam commissioning and testing. Next, we will proceed with installation and testing in other sections of SHINE.

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