A STACKED TRANSFORMER MODULATOR THAT DELIVERS HIGH VOLTAGE AT HIGH REP-RATE AND DUTY FACTOR*

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Abstract

A modulator has been built to drive the gun anode of the Tevatron Electron Lenses (TEL) at Fermilab. High voltage applied to the gun defines electron beam current in order for the TEL to perform beam-beam compensation in the Tevatron on each of the 36 (anti)proton bunches. Every bunch requires its own defined current, and the value of current for each bunch is different with each Tevatron "store". These requirements demand the modulator deliver a complex output voltage waveform with a high duty factor and high repetition rate exceeding 5 kV. The modulator described here utilizes a novel circuit topology employing 5 pulse transformers whose secondaries are connected in series to produce complex voltage waveforms played out repeatedly having peak voltages of 6 kV with average periodic rates up to 423 kHz and short bursts at 2.5 MHz. This paper describes the design approach taken to leverage the virtues of transformers for high rep-rates and duty factors while dealing with the adverse effects of parasitics to achieve speed. Design details and performance results are presented.

I. INTRODUCTION

The two TEL systems were proposed for compensating adverse beam-beam effects of colliding beams in the Tevatron [1]. Implementation of this compensation needs to be done on a bunch-by-bunch basis—whether on protons or antiprotons. This means that each of the Tevatron 36 (anti)proton bunches would pass through an electron beam of an appropriately defined current density. Electron current is generated by the electron gun following the relation: $I_{gun}=kV_{anode}^{3/2}$, where k is gun purveyance. This requires the gun anode driver (modulator) output a unique voltage for each of the 36 bunches. Bunches are spaced 395 ns apart.

The electron gun anode modulator needs to be essentially a 5 kV output (minimum), arbitrary waveform generator that transitions to different voltages at 395 ns intervals. The 36 bunches are grouped in three equally spaced bunch trains containing 12 bunches and a 2.3 μs abort gap. The pattern of defined voltage for one 12-bunch train and abort gap represents a defined "waveform". (A good waveform example is in Figure 8.) A waveform period is always 7.1 μs. The modulator is controlled to output a waveform with a unique positive voltage for each of the 12 bunches and typically "zero" volts during the abort gap. The pattern of bunch-by-bunch adverse beam-beam effects is nearly the same for each of the three bunch trains in the Tevatron. Therefore, the same voltage waveform is repeated three times every Tevatron revolution (21μs) to compensate all 36 (anti)proton bunches. Re-triggering the same waveform pattern every 7.1 μs (or even twice per Tevatron revolution) results in the production of high duty factor waveforms.

Modulator requirements are:

1. (Anti)proton bunches must encounter the same electron lens current every Tevatron revolution, whether it be zero or non-zero.
2. Applied gun voltage needs to be stable with time—low ripple (<<1%).
3. Output voltage 5 kVpp minimum.
4. Gun anode load is 60 pF.
5. (Anti)proton bunch transit time through the electron beam in the TEL is 6 ns. Exact requirements for dV/dt during this transit time are not exactly known, but several volts per ns is probably acceptable.

The Stacked Transformer Modulator step-changes to discrete voltage levels by controlling the drive to five pulse transformers with a common input DC voltage. It delivers stable, repeatable voltages that transitions to different values at regular time intervals. Its output is AC coupled that is then offset with respect to DC at the gun anode.

II. DESIGN OVERVIEW

The interest to pursue the use of multiple pulse transformers followed the line of reasoning that: 1) transformers lend themselves to high duty factor waveforms; 2) driving a number of transformers with their secondaries connected in series could "stack" voltage to a higher value; 3) pulse transformers offer fast rise times; 4) although transformers AC couple voltage, the output will be AC coupled anyway; and 5) there is an advantageous voltage doubling effect by driving them in a bipolar manner.

Figure 1 shows the circuit topology for this modulator built with five pulse transformers. Each transformer primary is driven by its own ground-referenced, H-bridge driver. The drivers are supplied by the common adjustable 0 to 800 Vdc source VIN. All H-bridge drivers are independently controlled. Voltage applied to each transformer need not necessarily change for every beam bunch at the 395 ns bunch spacing, but when H-bridges do switch, they do so at the same time. H-bridges are switched immediately after an (anti)proton bunch transits

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through the electron beam in order to allow the maximum settling time for the next bunch.

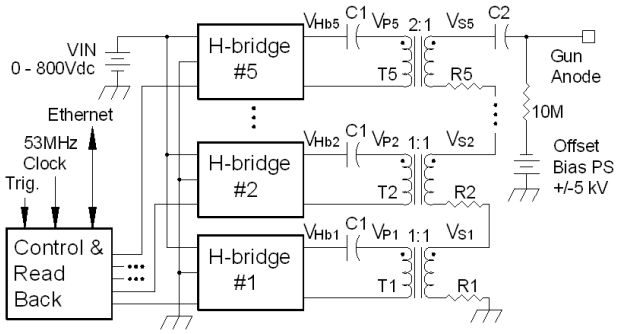


Figure 1. System block diagram.

There are only a few passive components at high voltage: transformer secondaries, series damping resistors and the output series capacitor, C2. The Offset Bias PS is external and controlled separately to align, voltage wise, the output waveform with the electron gun cathode.

The descriptions of waveforms are down loaded over Ethernet to the controller. A waveform description exists for each of the five transformers, and the modulator outputs a net voltage waveform. A description defines the H-bridge switch state at each of the 395 ns time intervals. Switching is synchronized with the Tevatron by way of the 53 MHz clock and first-turn trigger. Interface to the modulator is by way of the Fermilab ACNET control system.

The load is high impedance, but the switching rates are high enough that switching losses are non-trivial. The chassis is designed to direct forced air specifically to FET heat sinks, transformer cores and secondary side resistors.

III. TRANSFORMER DRIVE SCHEME

It is necessary that the modulator output voltage be variable so that each beam bunch encounters its own prescribed value of electron current to compensate it. Once the value of VIN has been determined for the maximum needed tune shift, it is set and remains fixed. It is not varied with time. Voltage must change to a different value quickly and settle in time for the next beam bunch, and this is performed by the H-bridge drive of transformers. The important aspects of this drive scheme are the combined use of bipolar drive and the primary series capacitor—C1 shown in Figure 1.

A. Bipolar drive

Each H-bridge delivers three different voltages to a primary. They apply VIN in either the positive direction, the negative direction or they apply a short across the primary. Employing a number of transformers enables a variety of discretely different output voltages when +/- VIN and 0 V are applied to the five transformer primaries in various combinations, since at any given time the output voltage is always the sum of the five secondaries.

When all the transformers are driven negative, the result is the minimum waveform voltage at the modulator output. When all are driven together positive, the result is the maximum waveform voltage. The difference between this waveform maximum and minimum depends on the value of VIN—call this value Vpp_max. This modulator has five transformers with two different turns ratios among them, so Vpp_max is

$$Vpp\_max = 2\times VIN\ (3 + 2\times(1/2)) = 8\times VIN.$$

Additionally, there are always 16 equally spaced discrete output voltages that can possibly be produced from 0 to Vpp_max by applying all possible drive combinations. Stated another way, knowing the desired value of Vpp_max at the output determines what the value VIN needs to be, and the settable voltage resolution within the waveform is Vpp_max/16 (or VIN/2).

B. Primary series capacitor, C1

The capacitor in series with the primary, C1, is beneficial for accomplishing a number of things. The primary is AC coupled, so C1 naturally averages out any voltage waveform across the primary, and the transformer is prevented from marching towards saturation. Additionally, the primary waveform becomes volts•seconds averaged plus and minus, so the core's B/H curve is more fully utilized. In this case, transformers were designed for (800V)×(2.4μs) = 1.9mV•s, but because of C1 we can get 3.8 mV•s out of them. The only caveat is that it takes time for steady state voltage to develop across C1. Therefore, to prevent saturation, switching is enabled first; then VIN is ramped up to voltage and slew rate limited.

Another benefit of C1 is DC blocking. Taking advantage of this, we make the H-bridge normally "off" state be –VIN. As switching commences, the capacitor voltage shifts in a manner to average out the voltage waveform, and the transformer output voltage becomes unipolar positive. The period of the C1 and primary inductance resonance is long relative to the 7.1 μs waveform, so voltage droop from C1 is small.

The modulator output is offset by the Offset Bias PS at the gun anode by an amount such that the minimum (or most negative) waveform voltage will be the gun cathode potential. Any positive voltage on the gun anode with respect to the cathode results in electron emission. We can construct high voltage, complex waveforms of arbitrary duty factor. The waveform's most negative voltage can be DC offset to that of the cathode, so the whole waveform is used to produce useful current. **Regardless of the waveform, the Stacked Transformer Modulator acts like a unipolar, DC referenced pulser.**

C. Example

This drive scheme is illustrated in Figure 2 showing waveform signals passing through two transformers. Voltage waveforms in (a) and (b) are voltages of transformers #1 and #2, respectively. The labels in the diagram titles correspond to the labeled signals in Figure 1. These waveforms are represented at steady-state condition. Transformers #3, #4 and #5 are assumed to be continuously driven off and will contribute no voltage to the output. The input voltage VIN is 800 Vdc in this example and represents a realistic value. Strictly for explanation purposes, the waveform period shown consists of ten equal intervals.

The Figure 2(a1) shows the three distinct voltages that an H-bridge can deliver to a primary. The waveform starts at time t(0) when transformer #1 switches from -800 V to 0 V. Producing this is H-bridge #1 switching from -800 V to a shorted condition. At t(1) H-bridge switches from a short to +800 V. H-bridge #1 does not switch again until t(4) at which time it returns to -800 V; this is the "normally off" state.

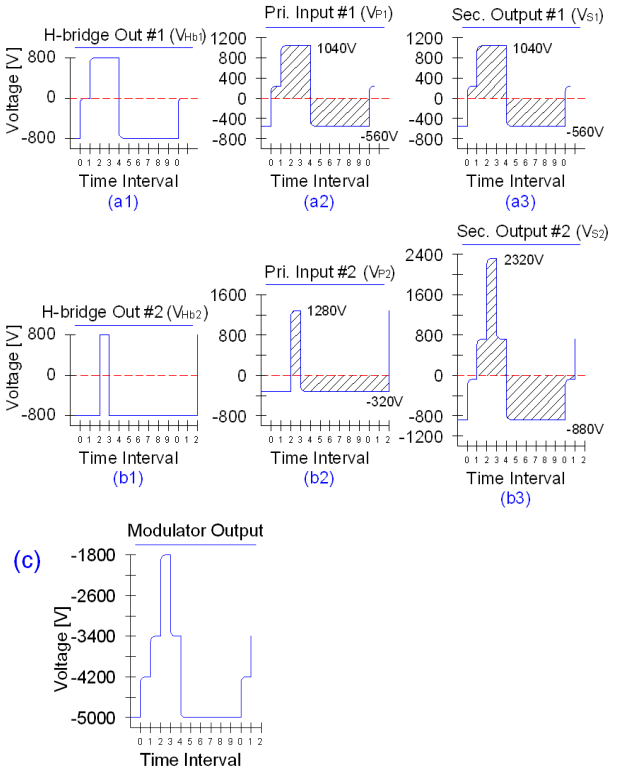


Figure 2. An example illustrating the way two 1:1 wound transformers can be driven to produce a 3200 Vpp output from an 800Vdc input.

Shown in Figure 2(b1), H-bridge #2 switches from -800 V to +800 V at t(2) and returns to -800 V at the next time interval t(3). This makes for a narrow pulse that contributes voltage to the output during the time that #1 is being held constant at the +800V.

The waveforms at Figure 2(a2) and (b2) are the voltages across the primaries and the shaded areas show how both waveforms are averaged about zero volts. The volts•seconds product is different for the two transformers, so the minimum and maximum absolute voltages are different at the two primaries. However, notice that the peak-to-peak voltage for both is the same, namely 1600 Vpp.

Figures 2(a3) and (b3) show the secondary voltages. The low side of secondary #1 is tied to ground, so (a3) is the same as (a2); however, (b3) is the sum of the output of two secondaries. Because #2 is switched to maximum voltage between t(2) and t(3) during the time that #1 is also at maximum, the result will be a 3200 Vpp waveform. Voltage at secondary #2 is AC coupled, so the waveform is averaged about zero volts as shown in (b3).

Figure 2(c3) is the modulator output that has been offset by -4120 V to presumably set the minimum voltage to equal the cathode voltage of -5000 V . Thus, two 800 V transformers each wound 1:1 have produced a waveform of 3200 Vpp. What is important for this application is electron current density each beam encounters as it passes through the TEL—current defined by gun anode voltage. Using multiple transformers and controlling the H-bridge timing, we can obtain different voltages at specific times with defined resolution. Because in this example VIN is assumed to be 800 Vdc, the settable voltage resolution is 800 V using transformers #1 or #2. Both of these are wound 1:1. If, instead, #4 or #5 were used the settable resolution would be 400 V, since these transformers are wound 2:1.

IV. DESIGN DETAILS

All design effort is in the interest to obtain at least 5 kVpp output having as fast a rise time as possible. (Fast rise time directly relates to the flattop dV/dt.) The major efforts in achieving these objectives went into the design of the transformers and to minimize and dissipate the power resulting from parasitic capacitance in several places.

A. Transformer parasitics modeling

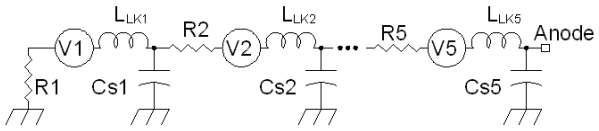


Figure 3: Secondary side parasitics model.

The deleterious effects of transformer parasitics add up in a hurry when stacking multiple, wound transformers in series. Tests were done to verify a good parasitics model of a pulse transformer by winding a sample core and comparing its pulse response to that of a RLC SPICE model using measured leakage inductance and secondary to primary capacitance and the damping resistor

calculated from the expression $R=2\times sqrt(L_{Lk}/Cs)$. Pulsing the transformer into an open circuit load, the series resistor value was adjusted to obtain critical damping. This simple RLC circuit was demonstrated to be a good parasitics model of a pulse transformer with the leakage inductance reflected to the secondary side.

This model was then used to construct a SPICE model of the entire secondary side circuit shown in Figure 3. **What is important about this topology is the value and placement of these resistors that make it possible to stack multiple pulse transformer secondaries in series and obtain a critically damped pulse response.** Success of this is revealed in the plot in Figure 9.

B. Waveform construction and switching rates

The need to deliver defined voltages at 395 ns intervals results in the construction of complex waveforms. Figure 2 illustrates the way multiple transformers contribute voltage to the modulator output waveform. A waveform of 7.1 μs duration contains 12 distinct voltages timed with beam bunches.

Effective compensation of a 12-bunch train requires voltages to possibly return to zero as many as three times in a waveform pattern, not just once—during the abort gap. A waveform is to be repeated three times every Tevatron revolution of 21 μs to compensate all 36 (anti)proton bunches. This means that voltages would be rising to kilovolts and returning to "zero" (the minimum waveform voltage) at potentially sustained average rates of: (1/21μs)×3×3 = 423 kHz. This significantly affects switching and transformer core losses. Switching bursts occur at (1/395ns) = 2.5 MHz.

C. Transformer design

Working with the parasitics model of Figure 3, it was desirable to keep transformer leakage inductance below 2 μH. Ceramic Magnetics, Inc. MN8CX core material was chosen for its combination of low loss and high mu at these switching rates, and transformers were sized for roughly 50 Watts worst case. Worst case was chosen to be 1.92 mV•s. A MathCAD spread sheet was used to iterate towards a design making tradeoffs between turns, turns ratios and core area.

All transformers have the same core area of 2.0 in^2. However, the winding spacing and insulation thickness are different from each other in an attempt to take advantage of the voltage grading of the five. Primaries are wound on Nomex® tightly wrapped on the ferrite core cylinder. Secondary insulation is a tight wrap of .010" Nomex® layers. All windings are #20 wire. Figure 4 show the wound transformer of the #4 assembly.

Table 1 lists the transformer parameters where: X is the transformer as per the numbering in Figure 1; Np and Ns are primary and secondary turns; Lp is primary inductance; L_{Lk} is leakage inductance measured on the primary side with the secondary shorted; Cs is secondary to primary capacitance; W_H is the physical height of the windings, where both the primary and secondary are the same; W_{Th} is the secondary insulation thickness; and Vc is the corona extinction voltage measured between secondary and primary with the primary grounded.

Secondary turns were wound to lay immediately over those of the primary which minimizes leakage inductance of transformers #1, 2 and 3. The windings of #4 and #5 are not 1:1 and could not be lined up in this manner, so leakage inductance was higher even though they have fewer turns.

One helpful expression used in iterating towards transformer designs is the calculation for leakage inductance, $L_{Lk} = 4\pi 10^{-7} Np^2 Aps/W_L$ (H) [2], where Aps is the area between primary and secondary. This shows that leakage inductance can be decreased by spreading windings apart. However, the effectiveness was found to diminish beyond a .2" turn-to-turn spacing.

Figure 4: H-bridge driver and transformer module assembly.

Table 1. Transformer parameters.

X	Np	Ns	Lp (μH)	L_{Lk} (μH)	Cs (pF)	W_H (in.)	W_{Th} (in.)	Vc (volts)
1	11	11	2130	2.13	42	2.25	.050	1400
2	11	11	2430	2.09	42	2.25	.030	1600
3	11	11	2076	2.28	34	2.0	.060	2500
4	10	5	1520	3.79	25	1.6	.080	3150
5	10	5	1520	3.75	22	1.6	.080	3000

D. Switching and transformer core losses

This modulator delivers no real power to a load. All dissipated power internally is a result of either switching losses in the H-bridge FETs, transformer core losses or charging and discharging secondary side parasitic capacitance. Resistor power dissipated from charging and discharging any capacitor is $C \bullet V^2 f$. Data from the SPICE model was used to calculate the power dissipated in resistors R1-5 of Figure 2 from the parasitics C_{S1}-C_{S5}. The total estimated power was ~650 W and distributed increasingly from R1 to R5.

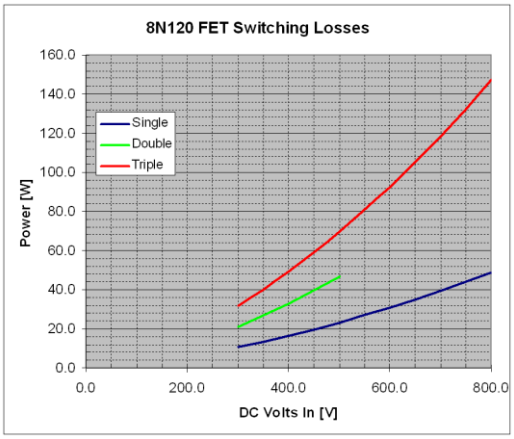
Figure 5 shows switching losses measured in both an H-bridge and a transformer core for three different switching rates: 141, 282 and 423 kHz at various input voltages. (Some data was not taken for the "Double", 282 kHz, switching rate.) "Single", "Double" and "Triple" refer to the number of full H-bridge switching cycles

every 7.1 μs; i.e., H-bridges switch VIN fully negative and positive at 141, 282 and 423 kHz as encountered in "complex" waveforms. The four H-bridge FETs are switched on and off equally in the three conditions.

E. Control

The embedded controller is an assembly of several PCBs. It contains a RCM3010 8-bit microprocessor core module from Rabbit Semiconductor that handles communications with the ACNET control system. H-bridge switching control logic is configured into Altera MaxII complex programmable logic (CPLD) ICs. Waveform descriptions are downloaded into the CPLDs. Codes are sent for each transformer and each switching time interval. Waveform switching is synchronized with the external 53 MHz Tevatron clock and are triggered every machine revolution.

(a)



(b)

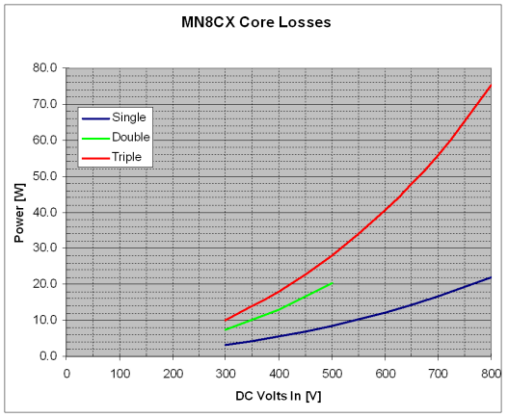


Figure 5. Measured switching losses at 141, 282 and 423 kHz; (a) in an H-bridge, (b) in a core.

Some monitoring is provided. Temperatures of the ferrite cores and a FET heat sink on every H-bridge board are monitored as are each H-bridge input DC current. H-bridges will trip off at adjustable over current limit values.

F. H-bridge hardware

The H-bridges need to switch quickly to allow for maximum settling time every 395 ns interval but avoid any shoot-through current with hundreds of volts applied. The MOSFETs chosen were IXYS IXZR08N120 that have rise and fall times of 5 and 6 ns, respectively, and delay times are only 4 ns. The dead time between turn off and turn on of the two FETs in branch is set to be 20 ns.

Individual H-bridges can be switched out of operation either remotely or upon detection of over current. Input voltage is disconnected, and freewheeling diodes clamp its output to 0 V.

H-bridge FETs receives individual TTL drive signals from the controller over 200 ohm terminated ribbon cable. The gate drive circuits employ a high voltage translator IC that has an isolation slew rate limit of 30 kV/μs. The mid points of both H-bridge branches will exceed this using these fast FETs when VIN is greater than 500 V. A simple passive RC network at the FET gates slows down, a little, the gates through the turn on region without adding much other delay. Voltage rise time including dead time is ~90 ns. For better or worse, this scheme was used fiber optics. Enclosing H-bridges in shielded compartments keeps noise out of all low level control circuitry. All control wiring and compartment shielding can be seen in Figure 7.

G. Mechanical construction and cooling

Components requiring cooling are the H-bridge FETs, the transformer cores and secondary side damping resistors. The H-bridge driver board and its transformer were made as a module to minimize lead inductance which also formed a common path for cooling. Module #4 is shown in Figure 4.

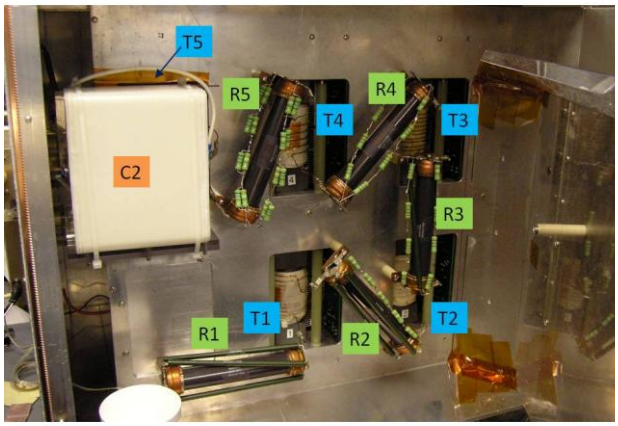


Figure 6. Secondary side resistors mounted in the rear of the chassis and their connections to secondaries.

The chassis positions three transformer assembly modules on top of the other two. See Figure 7. Located close behind are the secondary side resistors that have short leads between the secondaries. The secondary components are shown in Figure 6; the labeling corresponds to the designations in Figure 1.

For cooling, air is forced from the front of the chassis through the transformer assemblies to cool both the FET

heat sinks and the transformer cores then past the damping resistors. One 300 CFM fan was used in the chassis. The chassis inside front view is shown in Figure 7.

Figure 7. Inside front view showing 6 enclosed bays.

V. RESULTS

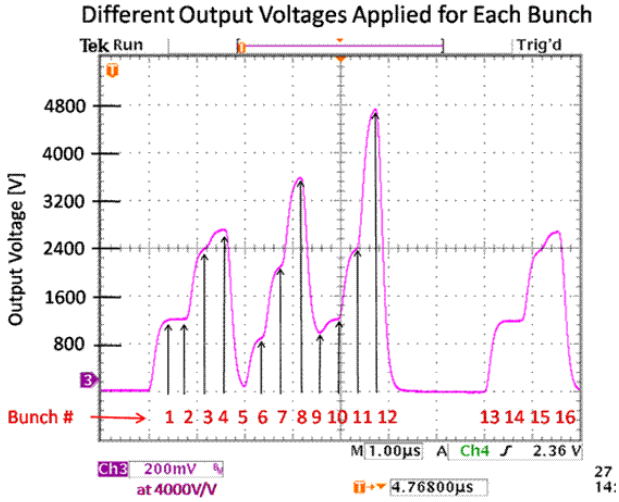


Figure 8: High voltage, high duty factor and rep rate output. Sketched in are bunches illustrating their alignment with the modulator output. A 2.3 µs gap occurs after bunch #12; the waveform repeats at bunch #13.

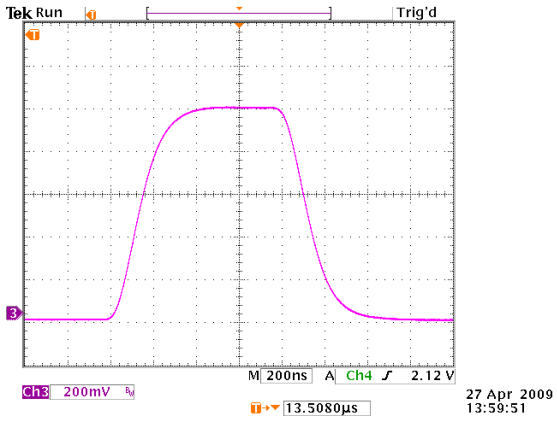


Figure 9. 4.0 kV pulse output; input is 500 Vdc.

Figure 8 shows the modulator output of a complex waveform created to compensate protons in Tevatron store #5162. Voltages transition to different levels for every one of the 12 bunches with the exception of #2 that is the same voltage as #1. Input voltage VIN is set to 600 V, and the maximum voltage produced is 4800 V at bunch #12. (This waveform is shown without bias offset voltage applied at the output.) Not observable at this time scale are the 50 ns windows of time the voltages settle to a constant worst case slope of 3V/ns in the interval after switching to different voltages. The voltage slope is dead flat after 500 ns if held constant as can be seen in Figure 9. Droop for very wide pulses arises from the minimum L/R time constant of 400 µs for all the transformers.

Figure 9 shows a single, narrow pulse that reveals the critically damped output response. All transformers are switched positive together for two time intervals (790ns). The input is 500 Vdc. Rise time, 10 – 90%, is 200 ns.

There exists a voltage-frequency trade off that should be made with regards to switching an H-bridge on and off at 423 kHz with input DC voltages above 700 V for sustained periods of time. MOSFET Junction temperatures are calculated to be ~105 °C when VIN is 800 V switching at this rate, but decreases as expected with the square of voltage and linearly with switching rate—see Figure 5(a).

VI. CONCLUSION

The Stacked Transformer Modulator has been installed that enables the TEL2 to provide beam-beam compensation of any (as well as all 36) (anti)proton bunches when desired. This modulator functions as if it were a type of high voltage arbitrary waveform generator. Its multiple transformer topology enables it to deliver high duty factor, high rep-rate waveforms that can be repeated every 7.1 µs having output voltages up to 6.4 kVpp and 16 definable voltage levels proportional to a DC voltage input.

VII. ACKNOWLEDGEMENTS

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