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Recent developments in fast timing ASICs for particle physics and medical imaging

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Summary. — This paper will cover recent developments and trends in ASICs designed by Weeroc and its affiliated laboratory, OMEGA (IN2P3/CNRS/Ecole Polytechnique), for medical imaging and particle physics applications. Two categories of ASIC will be reviewed: ASICs for medical imaging (*e.g.*, TOF-PET) which have been designed for obtaining the lowest CTR (sub 100 ps RMS) and ASICs in particles physics which are driven by readout of fast silicon sensors in the HL-LHC upgrade program.

1. – Introduction

Petiroc2A is a 32-channel SiPM readout ASIC, which has been designed for applications requiring precise timing and energy measurement such as time-of-flight positron emission tomography. Petiroc2A has been co-developed by Weeroc and Omega specifically for addressing the medical imaging market. This chip has been designed in AMS BiCMOS 0.35 um process.

ALTIROC1 has been specially developed by the Omega laboratory in collaboration with SLAC and SMU for ATLAS HGTD within the HL-LHC upgrade framework. This chip has been designed using TSMC 130 nm CMOS process. The sensor readout for this ASIC is LGAD.

2. – Petiroc2A

2˙1. *Description.* – Petiroc2A [1] is designed to be DC-coupled directly to the detector and external resistors can be added at each ASIC input in order to reduce the line impedance (*e.g.*, 50 Ohm). The high-bandwidth pre-amplifiers and time discriminator can be configured to accept both negative and positive polarity input signals. For correcting the SiPM array gain non-uniformity, each channel is provided with an input DAC, capable of trimming SiPM overvoltage up to 1 V individually for each channel.

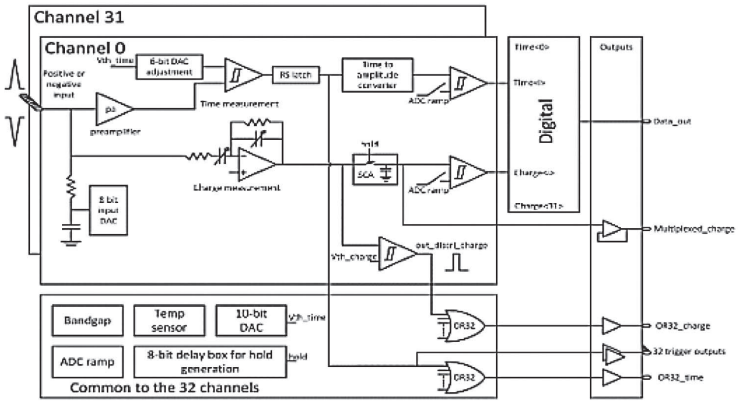

Fig. 1. – Petiroc2A block diagram.

The timing path is obtained directly from the pre-amplifier and the time discriminator. The resulting time triggers are sent either to the ASIC pad (in total 32 trigger outputs plus an OR output) or towards the internal time-to-amplitude converter (TAC) for time stamping the incoming photons.

In parallel with the timing path, a semi-Gaussian shaper with variable gain and shaping time is available for measuring the energy. The shaper signal is sent to the Track/Hold stage for charge measurement through the internal ADC or externally via a multiplexed analog output. Additionally, a charge trigger is also available for the charge measurement path. The digital core is composed of a coarse time counter, Wilkinson ADC and readout management. The readout is performed on demand and asynchronously by a control signal initiated by a FPGA.

The time measurement system here is composed of a 9-bit Coarse Time and a 10-bit of Fine Time for each channel. The Fine Time is provided by the internal Wilkinson ADC, which converts the data from TAC. The resulting binning of the Fine Time is around 30 ps.

The Charge measurement is relatively straightforward where Wilkinson ADC is also used to perform the digital conversion of the analog signal stored in the shaper Track/Hold cells. The user can set internally the delay between the time trigger and the shaper's peak in order to convert the maximum amplitude of this shaper.

The 9-bit Corse Time, Hit information for charge trigger, 10-bit Charge information and the 10-bit Fine Time are sent through a serial LVDS link running at 80 MHz. When running with full digital conversion, the ASIC is expected to be able to process up to 40 k events/s. The architecture of Petiroc2A is shown in fig. 1.

2˙2. *Experimental measurements.* – After the characterisation phase, Petiroc2A has been measured further with detectors. The measurements have been focused on the Petiroc2A behavior with various SiPM models from manufacturers, such as FBK, Hamamatsu and Sensl. The scintillators used during the measurements are mostly LSO:Ce,Ca with dimensions ranging from $2 \times 2 \times 3\,\mathrm{mm}^3$ to $3 \times 3 \times 20\,\mathrm{mm}^3$. Most of the measurements with isotope were done with Na22. CTR measurements have been performed with either oscilloscope or internally by TDC of Petiroc2A. For SPTR, a low jitter laser source and an oscilloscope were used for the measurements.

SPTR measurements have performed using a low-jitter laser source and several SiPMs of various pixel sizes and active area. The best result (fig. 2) was obtained from FBK

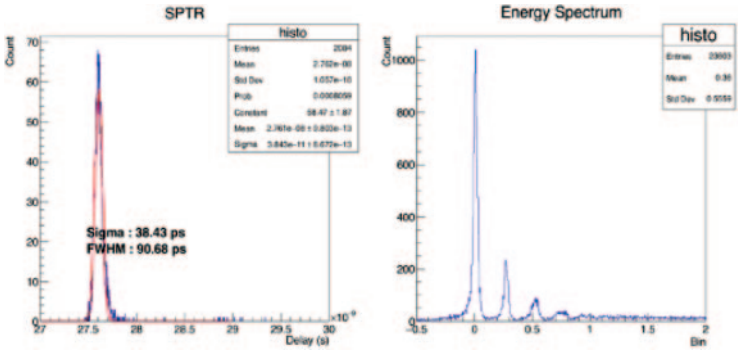

Fig. 2. – Petiroc2A SPTR with FBK NUV $1 \times 1\,\mathrm{mm}^2$ SiPM. The obtained value is 90.7 ps FWHM.

NUV SiPM, which is a relatively small device ($1 \times 1\,\mathrm{mm}^2$). The SPTR obtained with this device is about 90.7 ps FWHM. SPTR values tend to get better with smaller size SiPM. For example, when measured with SiPM from Hamatmatsu, the SPTR results is better with the $1.3 \times 1.3\,\mathrm{mm}^2$ device (MPPC 1350PE) compared to the $3 \times 3\,\mathrm{mm}^2$ device (3050CS).

CTR measurements (fig. 3) were performed for Petiroc2A trigger outputs by using a high-bandwidth oscilloscope (analog mode) and also the ASIC's internal TDC (digital mode). For this analog setup, a Na22 source, $2 \times 2 \times 5\,\mathrm{mm}^3$ LSO:Ce,Ca scintillator and FBK NUV-HD $4 \times 4\,\mathrm{mm}^2$ SiPM were used. The coincidence events are selected within the 511 keV spectrum. The measured CTR is about 85.5 ps FWHM.

Similar measurements under the same setup were performed using internal TDC of Petiroc2A (fig. 4). The obtained value for CTR is 127.3 ps FWHM. This difference indicates that internal TDC provides added noise to the measurement. Similarly, the non-linearity of the TDC does degrade the CTR measurement results.

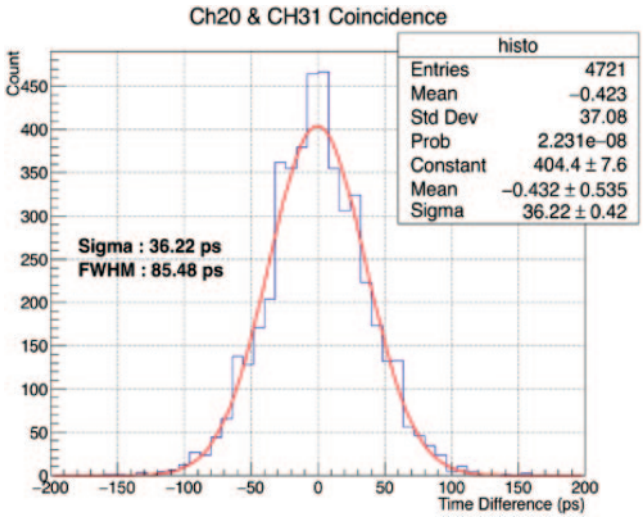

Fig. 3. – Petiroc2A CTR measured with FBK NUV-HD $4 \times 4\,\mathrm{mm}^2$, 40 um and $2 \times 2 \times 3\,\mathrm{mm}^3$ LSO:Ce,Ca in analog mode. The obtained CTR value is 85.5 ps FWHM.

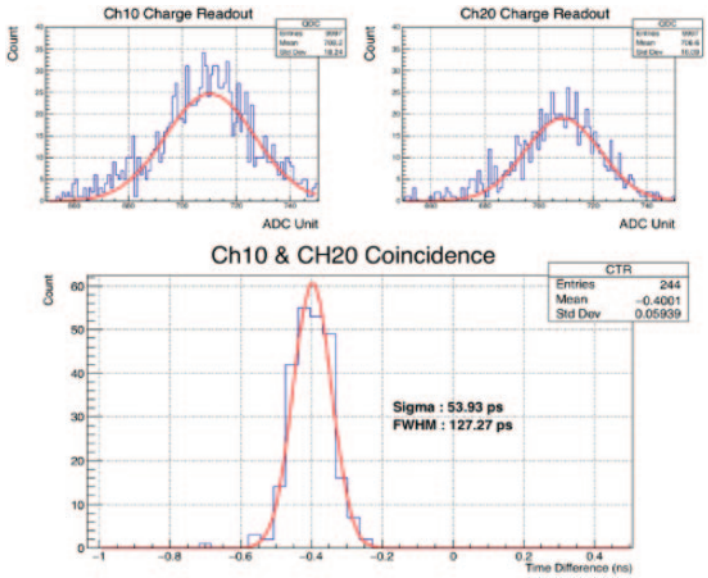

Fig. 4. – Petiroc2A CTR measured with FBK NUV-HD $4 \times 4\,\mathrm{mm}^2$, 40 um and $2 \times 2 \times 3\,\mathrm{mm}^3$ LSO:Ce,Ca using internal TDC. The obtained CTR value is 127.3 ps FWHM.

Additionally, the CTR performance of this ASIC has been also measured with positive and negative SiPM output. For example, the CTR measurements for LSO:Ce,Ca of $3 \times 3 \times 20\,\mathrm{mm}^3$ in dimensions and Hamamatsu MPPC S13360 3050PE $3 \times 3\,\mathrm{mm}^2$ SiPM yield a value of 222.5 ps FWHM for the negative SiPM signal. Using the same setup, CTR for positive polarity signal is about 235.05 ps FWHM.

3. – ALTIROC1

3˙1. *ASIC description.* – ALTIROC1 [2] has been designed in CMOS 130 nm to read out a 5×5 LGAD matrix with a complete on-pixel readout. The analog part consists of a 1 GHz RF preamplifier followed by a high-speed discriminator, which are both critical elements for the overall electronics time performance. Each discriminator is followed by a Time-Of-Arrival (TOA) and a Time-Over-Threshold (TOT) TDC as well as by a SRAM memory to store the digitized data. The TOA is digitized over 7 bits with a bin of 20 ps

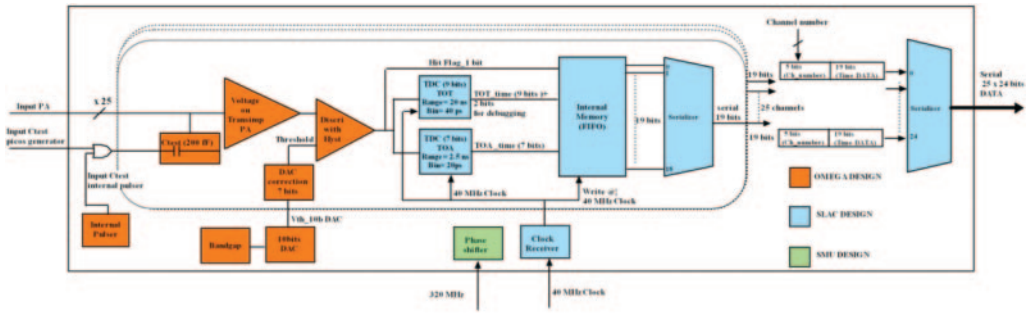

Fig. 5. – ALTIROC1 block diagram.

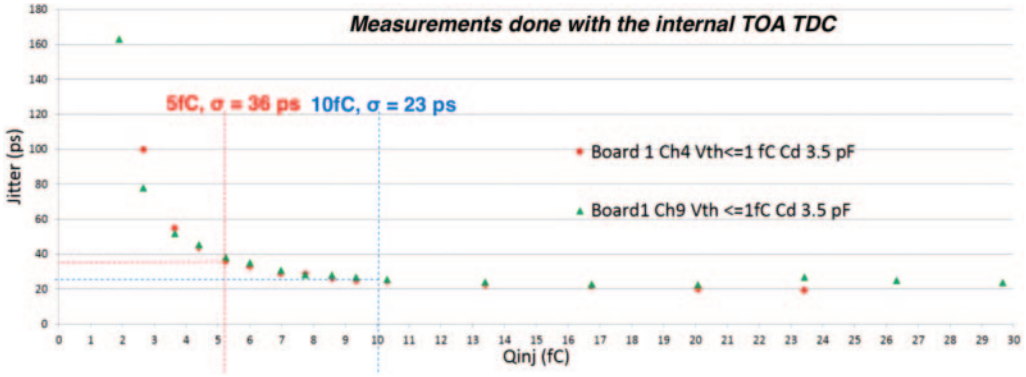

Fig. 6. – ALTIROC1 jitter measurement.

and is done within a 2.5 ns window centred on the bunch crossing. A Vernier delay line configuration has been chosen to achieve the 20 ps quantisation step. The conversion is initiated only upon signal detection, enabling power saving. The TOT measurement is digitized over 9 bits with a bin of 40 ps. The TDC employs an additional coarse delay line for extending the range to 20 ns while the Vernier delay line (identical to the one used in TOA TDC) provides the high resolution of 40 ps. The total power consumption for both TDCs is 1.1 mW/channel assuming a maximal channel occupancy of 10%. The memory is also custom-designed to minimize the power dissipation to less than 0.5 mW/channel with a 10% occupancy. It has a width of 19 bits and a depth of 400 columns to provide the 10 us L0 latency.

This chip is currently in the second prototype iteration with minor modifications, ALTIROC1_V2 and it has been received in June 2019. The block diagram of this chip is shown in fig. 5.

3˙2. *Experimental measurement.* – One of the main challenges of this ASIC is to maintain a reasonable low jitter especially when TOA is converted internally. As shown in fig. 6, the jitter is relatively reasonable at 23 ps for 10 fC of the injected charge.

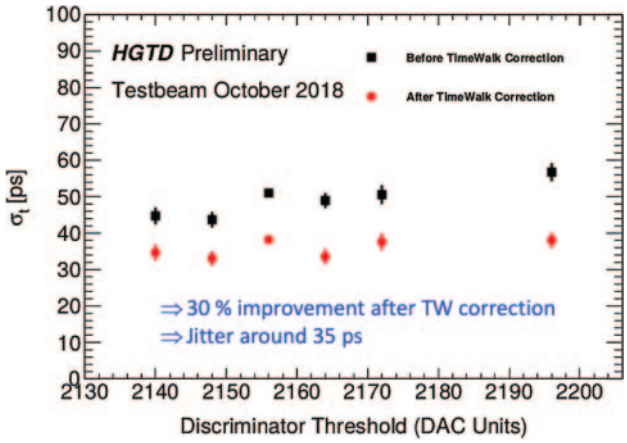

Fig. 7. – ALTIROC0 jitter measurement from testbeam.

A test beam has been conducted with previous iteration of ALTIROC (ALTIROC0_V2). After timewalk correction, the jitter is quite reasonable at 35 ps as shown in fig. 7.

4. – Conclusion

Petiroc2A and ALTIROC1 are some of the recent ASICs developments at Weeroc and Omega, following the demand of timing measurements stemming from medical imaging and particle physics experiments requirements. Petiroc2A has demonstrated the capability of reading out SiPM in a single device or also a complete array. Additionally, this ASIC has a reasonable timing performances as demonstrated by the measured CTR values of 85.5 ps FWHM for $2 \times 2 \times 3\,\mathrm{mm}^3$ LSO:Ce,Ca and FBK NUV-HD $4 \times 4\,\mathrm{mm}^2$, 40 um SiPM. The nearly similar CTR values for both input polarity emphasize the flexibility offered by this ASIC. On the other hand, ALTIROC1 and its various iterations have shown that this ASIC is capable of delivering required performances for ATLAS HGTD. The next iteration of this chip integrating a very dense digital part for data processing, ALTIROC2, is expected to be taped out in 2020.

REFERENCES

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[2] Seguin-Moreau N. *et al.*, *ALTIROC1, a 25 pico-second time resolution ASIC for the ATLAS High Granularity Timing Detector (HGTD)*, *TWEPP 2019, Santiago de Compostela, Spain, 2 September–6 September 2019.*