ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP27

THE DEVELOPMENT OF NEW BPM SIGNAL PROCESSOR AT SSRF*

M. J. Zhang[1], Shanghai University, Shanghai, China
[1]also at Shanghai Institute of Applied Physics, CAS, Shanghai, China
L. W. Lai†, Y. M. Zhou, Y. B. Yan, Shanghai Advanced Research Institute, CAS, Shanghai, China
H. Jang[2], S. L. Wang[2], Nanchang University, Jiangxi, China
[2]also at Shanghai Advanced Research Institute, CAS, Shanghai, China

Abstract

A BPM signal processor has been developed for SSRF since 2009. It composed of Virtex5 FPGA, ARM board, and 4 125MSPS sampling rate ADCs. Since then, electronic technology has made significant progress. Such as Zynq UltraScale+ MPSoC FPGA contains both hard-core ARM and high-performance FPGA, and ADCs with a sampling rate of 1GSPS have been applied in mass production. A new BPM processor with Zynq UltraScale+ MPSoC FPGA and 1GSPS ADCs is under development at SSRF. Due to the application of new technologies, the processor performance will be significantly improved. The new processor can also meet the needs of ultra-low emittance measurement for the new generation of light sources. This paper will introduce the design of the processor and the relative tests.

INTRODUCTION

The Shanghai Synchrotron Radiation Facility (SSRF) is a high-performance electron storage ring with a circumference of 432 meters and an energy of 3.5 GeV. It operates with a harmonic number of 720, a cyclotron frequency of 693.964 kHz, and a radio frequency of 499.654 MHz. SSRF is recognized as one of the leading medium-energy light sources worldwide, delivering exceptional performance in its class [1].

SSRF early adoption is the third generation BPM processor Libera series launched by IT companies, it has high resolution, high reliability, a large number of users, convenient technical communication and many other ad vantages. In the construction and upgrading of a new generation of accelerators, SSRF has developed a new digital BPM signal processor with independent intellectual property rights, and its performance has reached the international advanced level. The digital BPM signal processor is based on the embedded sub-motherboard structure of FPGA+ARM, equipped with different front-end ADC sub boards to adapt to different applications, there are four channel signal input, the center frequency is 500 MHz, 16 bits ADC, its the maximum sampling rate is 125 MSPS and bandwidth is 650 MHz. The beam test results of the processor on the storage ring show that the resolution of TBT reaches 230 nm, the resolution of SA data reaches 78 nm, the resolution of 10-minute closing orbit is 57 nm, the temperature change of 80 hours is 1.2 degrees, and the horizontal and vertical slow drift is less than 0.4 microns. At present, it has been used in batch in SSRF, SXFEL, DCLS, Brazil light source linear accelerator, the number of about 200 units. Table 1 describes the main operational parameters of SSRF.

Table 1: Main Parameters of the SSRF

Parameter	Value
Perimeter	420 m
Beam energy	3.5 GeV
RF frequency	499.654 MHz
Harmonic number	720
current	240+0.5 mA
Emittance	3.9 nm/rad

Beam orbit stability is critical for the operation of synchrotron radiation sources, with drift being the primary factor affecting orbit stability. When beam position monitors (BPMs) measure beam position, slow drifts are introduced due to factors such as ambient temperature, humidity, pressure, and electromagnetic fields, which arise from channel inconsistencies. These drifts degrade the accuracy and resolution of the data, leading to inaccurate BPM feedback. Currently, two main approaches are employed for drift compensation: pilot tone and switching. Based on a survey of major scientific facilities worldwide, pilot tone compensation is used in Elettra 2.0 [2], Diamond-II, SLS, HEPS, and BEPC II, while switching is implemented in NSLS-II, Sir ius, HEPS, and IT Libera. SSRF has opted for the pilot tone compensation method due to its effectiveness in eliminating channel inconsistencies, and has developed a new generation of digital BPM signal processors to enhance performance.

NEW DIGITAL SIGNAL PROCESSORS

SSRF has upgraded the electronics for universal beam measurements, achieving a sampling rate of 117.28 MHz, and developed a new generation digital backboard based on the latest system-on-chip FPGA (Zynq UltraScale+ MPSoC) architecture. This new design incorporates 8 GB of PL DDR memory and offers more versatile external interfaces. The RF front-end board has also been upgraded with the addition of a pilot tone to enhance orbit stability. Currently, the hardware integration, FPGA, and software development have been completed, and corresponding pilot function tests and data analysis are underway in both the laboratory and accelerator facility. The primary design of the BPM electronics includes an RF analog front-end

* This work was support by the National Natural Science Foundation of China (Grant No. 12175293). Youth Innovation Promotion Association, CAS (Grant No. 2019290), Outstanding member of the Youth Innovation Promotion Association, CAS, SHINE R&D and project.
† Corresponding author: lailw@sari.ac.cn

ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP27

board and a digital signal processing motherboard. As detailed in Table 2, the processor features the latest generation FPGA as its core, significantly boosting processing performance. Additionally, with 8 GB of PL DDR memory, the data caching capacity has been greatly enhanced.

Table 2: Processor Specifications

Parameter	Value
Channels	4
Bandwidth	650 MHz
ADC bits	16
Max ADC rate	125 MHz
FPGA	Xilinx ZCU15EG
Clock	Ext./Int.
Trigger	Ext./Self/Period
PL DDR4	8 GB
GPIO	12
Software	Arm-Linux/EPICS

Figure 1 shows the pictures of the processor, the blue is ADC board and the green is digital signal processing baseboard.

Figure 1: Picture of processor.

Pilot Tone

To verify the feasibility of the pilot tone compensation scheme, an Elettra eBPM analog front-end was acquired for experimental testing. Figure 2 presents the block diagram of the front-end, which includes the following com ponents: a low-pass filter, a high reverse-isolation com biner for the pilot tone, a band-pass filter, a variable attenuator, a low-noise amplifier, and a low-noise PLL for pilot tone generation.

Figure 2: Elettra eBPM analog front end [3, 4].

In the laboratory, a vector signal source is used to generate analog signals, which are then input into the Elettra eBPM analog front-end and coupled with the pilot tone. After filtering, amplification, and attenuation, the four signals are fed into the new BPM signal processor. The pro cessed signals from the prototype show excellent compensation performance, and the signal-to-noise ratio (SNR) of the Elettra eBPM analog front-end has been analyzed using a spectrum analyzer, demonstrating the effectiveness of the system.

Rf Analog Front End

We developed a new RF analog front-end with integrated pilot functions and ADC board connectivity. The design features six ports: four AD signal inputs, one clock input, and one pilot tone output. The pilot tone is generated by the front-end board's PLL, with frequency and amplitude controlled by the LMX2541 and PE43711 chips, respectively. The processor's sampling clock can be sourced either externally via the clock port or internally from a crystal oscillator. Figure 3 illustrates the structure of the RF front-end.

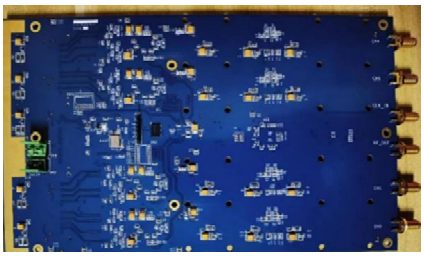

Figure 3: ADC board with RF analog front end.

The SSRF cyclotron frequency is 693.969 kHz, with an RF frequency of 499.654 MHz, exactly 720 times the cyclotron frequency. The processor's sampling rate is set at 117.2799 MHz, or 169 times the cyclotron frequency. After anti-aliasing and bandpass filtering, the BPM signal produces a 30.5344 MHz RF signal via frequency shifting. The pilot tone generated by the analog front end must be near the RF center frequency for effective compensation, positioned between harmonics of the cyclotron frequency. In the test, a pilot tone of 501.538 MHz was used, yielding a 32.40 MHz RF signal after undersampling. Figure 4 shows the input pilot and beam coupling signals.

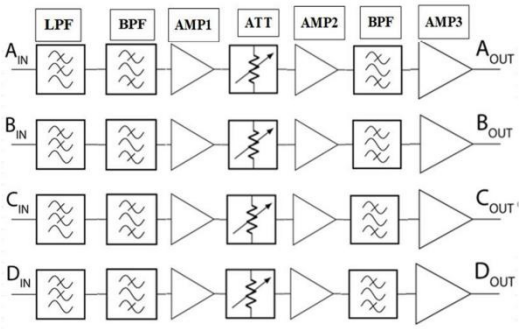

Figure 4: Block design of RF analog front end.

DIGITAL SIGNAL PROCESSING

To calculate the beam position, the signal amplitudes of the four channels are usually extracted and brought into the

ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP27

classical difference and ratio equation, and the equation will be changed by introducing pilot compensation [3]:

$$X = L \times \frac{(A_C/A_P + D_C/D_P) - (B_C/B_P + C_C/C_P)}{A_C/A_P + B_C/B_P + C_C/C_P + D_C/D_P}; \quad (1)$$

$$Y = L \times \frac{(A_C/A_P + B_C/B_P) - (C_C/C_P + D_C/D_P)}{A_C/A_P + B_C/B_P + C_C/C_P + D_C/D_P}. \quad (2)$$

There L is coefficient of channel, A_C, B_C, C_C, D_C are the amplitudes of the measured carrier and A_P, B_P, C_P, D_P are the amplitudes of the pilot tone.

The digital signal algorithm processing module mainly includes RF front-end processing, undersampling, digital down conversion (DDC), multistage filter extraction and so on. Among them, DDC is the key part of digital signal processing, Figure 5 is the program block diagram of the algorithm.

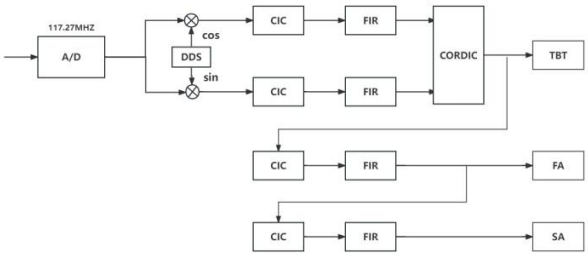

Figure 5: DDC of quadrature demodulation.

After filtering and amplifying the four-channel signal from the BPM probe via the RF front-end, the signal's center frequency is around 500 MHz with a 20 MHz band width. This high-frequency narrowband signal is under sampled at 117.2799 MHz by a four-channel 16-bit high speed ADC, shifting the spectrum to an intermediate frequency (IF) of 30.54 MHz, with the pilot signal at 32.40 MHz. After A/D conversion, the input signal undergoes quadrature mixing with the local oscillator signal generated by a direct digital synthesizer (DDS). The resulting I/Q de modulated signal is filtered through a 13-stage CIC filter, followed by a 13-stage FIR filter. The rate is reduced to the cyclotron frequency of 694 kHz, with a bandwidth of ap proximately half the cyclotron frequency range. The final calculated signal amplitude is used in difference and ratio formulas to compute the turn-by-turn beam position data. The signal is further filtered and extracted to a range between 50 kHz and 10 Hz, providing both fast feedback (FA) and slow acquisition (SA) data.

EXPERIMENTAL MEASUREMENT

TBT

The signal is directly acquired by the BPM signal processor without compensation, and after digital processing in the FPGA, the rate is reduced from 499.654 MHz to 694 kHz, producing turn-by-turn (TBT) data. The beam position is then calculated, with horizontal and vertical resolutions of 0.748 μm and 0.857 μm, respectively. Figure 6 il lustrates the relative position deviation.

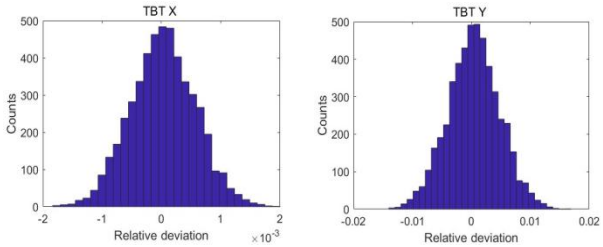

Figure 6: TBT position relative.

The vector signal source outputs a 499.654 MHz analog signal, which is coupled with the pilot tone and then pro cessed through the analog front-end before being input into the FPGA for digital signal processing. This yields compensated TBT position data at a rate of 694 kHz. The horizontal and vertical resolutions are 0.392 μm and 0.496 μm, respectively. Figure 7 displays the relative position deviation.

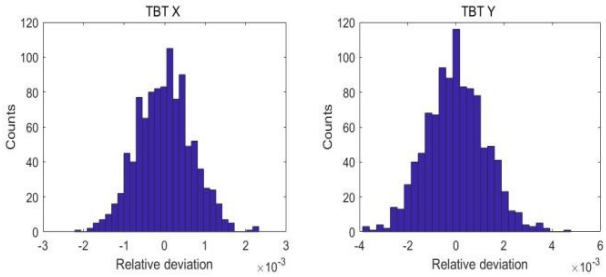

Figure 7: TBT position compensation relative.

FA

The fast acquisition (FA) data is continuously filtered and down-sampled, reducing the original data rate from 694 kHz to approximately 10 kHz. This process results in a horizontal resolution of 86 nm and a vertical resolution of 93 nm. Figure 8 shows the relative position deviations.

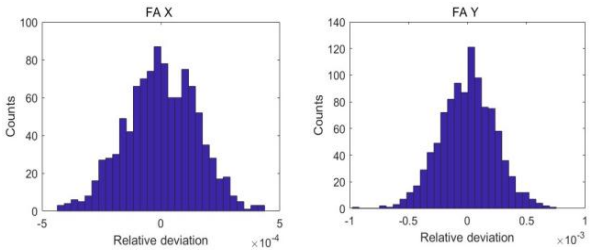

Figure 8: FA position compensation relative.

CONCLUSION

Based on the pilot compensation scheme, SSRF developed a new BPM digital signal processor prototype with integrated pilot functions, building on their existing self developed BPM signal processor. Equipment testing and data analysis conducted in the laboratory and storage ring have demonstrated a significant improvement in beam position resolution.

ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP27

REFERENCES

[1] http://www.ssrf.ac.cn

[2] G. Brajnik, S. Carrato, S. Bassanese, G. Cautero, and R. De Monte, "Pilot tone as a key to improving the spatial resolution of eBPMs", *AIP Conf. Proc*., vol. 1741, p. 020013, 2016. doi:10.1063/1.4952792

[3] G. Brajnik, S. Carrato, S. Bassanese, G. Cautero, and R. De Monte, "A Novel Electron-BPM Front End With Sub-Micron Resolution Based on Pilot-Tone Compensation: Test Results With Beam", in *Proc. IBIC'16*, Barcelona, Spain, Sep. 2016, pp. 307-310. doi:10.18429/JACoW-IBIC2016-TUPG02

[4] G. Brajnik, S. Bassanese, G. Cautero, S. Cleva, and R. De Monte, "Integration of a Pilot-Tone Based BPM System Within the Global Orbit Feedback Environment of Elettra", in *Proc. IBIC'18*, Shanghai, China, Sep. 2018, pp. 190-195. doi:10.18429/JACoW-IBIC2018-TUOC01