Pixel Readout Electronics in Honeywell SOI CMOS

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Abstract

Our aim is to design radiation-hard front-end electronics for pixel detectors at the Large Hadron Collider. The anticipated high radiation and collision rate environment at LHC places demanding requirements on the technology used. The circuits have to operate close to the beamline for several years without serious degradation of their parameters. The expected total radiation doses are up to 100Mrad Gamma and 10^{15} equivalent n/cm^2. We have investigated the suitability of the Honeywell 0.65μm_{Leff} SOI CMOS technology for front-end electronics of LHC experiments. To this purpose we have measured the DC, AC and noise parameters of NMOS and PMOS transistors built in this technology before and after irradiation with gammas from Co^{60} for a total dose of 55Mrad. All devices remained fully functional after irradiation, with no anomalous behaviour.

We have implemented in this technology the front-end readout system for a 22x32 pixel detector array with square pixels of (125μm)^2. The architecture is identical with the PSI31 chip fabricated in DMILL technology [1].

1. TECHNOLOGICAL ASPECTS

Honeywell has developed 0.65μm_{Leff}, 0.55μm_{Leff} and 0.28μm_{Leff} SOI CMOS technologies called RICMOS IV for radiation hard applications. The 0.65μm_{Leff} process has been optimized for designs operating up to 5V whereas the 0.55μm_{Leff} process supports low voltage operation up to 3.3V. The 0.28μm_{Leff} is a brand new development and will not be discussed in this paper. In the technology investigated the transistors are fabricated on full dose SIMOX wafers. The BOX thickness and Epi thickness amount to 370nm and 230nm respectively. A schematic diagram of an inverter designed in this technology is shown in Fig. 1. N and P wells are implanted to create a partially depleted polysilicon gate surface channel for NMOS and a buried channel for PMOS. The structure of N and P transistors are identical; they differ only in doping profiles. To eliminate latch-up the N and P transistors are fully isolated using BOX and CVD oxide refilled shallow trenches, which are self-aligned to the active areas and the transistor body. The active area is surrounded by body-tie which prevents the transistor from the kink effect and floating body effects. Improved LDD engineering has also been implemented in order to reduce the lateral drain electric field and to prevent the parasitic bipolar transistor from conducting. The drain and source nodes extend down to BOX to

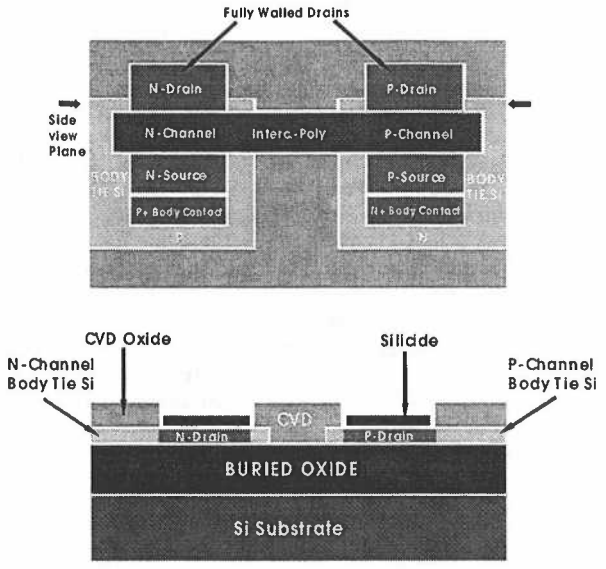


Fig. 1. Top view and cross-section of an inverter in RICMOS IV technology

reduce the parasitic capacitance on these nodes. To further reduce the parasitic capacitance on the drain the walled drain option can be used. The body contact can be entirely integrated in the source contact without the need for any additional area. These features increase the density of the circuits. The most significant advantage of the technology over other radiation-hard technologies is the availability of standard 3-layer metal or optional 4-layer metal for interconnections.

For analogue design RICMOS IV offers different passive elements:

- low value resistors with the sheet resistivity of 2.5Ω/sq., 30Ω/sq. and 100Ω/sq.
- high value resistors where the sheet resistivity can be chosen between 1000Ω/sq. and 5400Ω/sq.
- linear capacitors with good voltage coefficient and a high capacitance of 2fF/μm^2.
- metal fuses for redundancy repair

2. PRODUCTION OF CHIPS

We have submitted two designs in this technology:

- a test chip containing all important building blocks of the pixel detector readout, various transistors and preamplifiers for noise studies and irradiation tests, as well as comparators to study the matching of the transistors before and after irradiation.

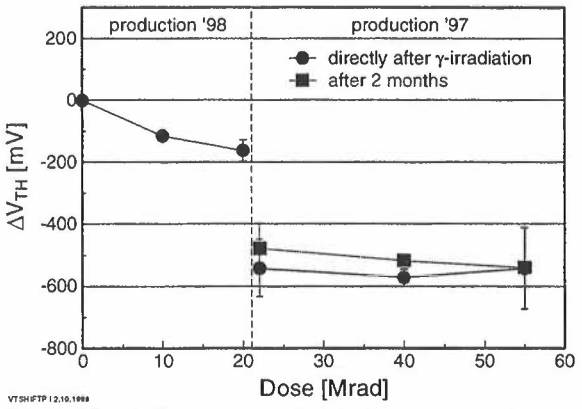


Fig. 2. Front channel threshold shift for PMOS

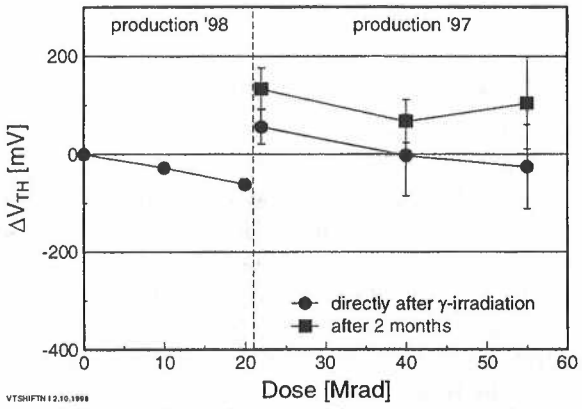


Fig. 3. Front channel threshold shift for NMOS

- a readout chip for a pixel detector array consisting of 22 x 32 cells.

We produced the chips in enhanced technology in an engineering run (10 wafers). The runtime was about 16 weeks. The chips were delivered by mid August and they have been under test since then.

3. RADIATION HARDNESS STUDIES

3.1 Irradiation Procedure

To investigate the radiation hardness of SOI technology a Co^{60} source with 1.1 MeV and 1.3MeV photons was used. We performed two irradiations:

- In '97 several transistors from process monitor bars have been irradiated with different dose rates to obtain total doses of 22Mrad, 40Mrad and 55Mrad. The irradiation was carried out within 99 hours for all transistors simultaneously. (Irradiation tests below 20Mrad were performed by the manufacturer Honeywell [2]). The results of the irradiation showed that the radiation hardness of PMOS should be improved. Honeywell has realised such an improvement.
- In September '98 we irradiated transistors from the latest wafer run, carried out in the enhanced technology. Using again different dose rates over a period of 33 hours. We have obtained total doses of 10Mrad and 20Mrad.

Irradiation to higher doses will be continued.

During the irradiation all devices were packed in an aluminium box in an argon atmosphere to avoid chemical reactions with the surfaces by aggressive gases like O_3. We irradiated the devices under analogue and digital biasing. In the analogue case the transistors were connected in diode configuration with the drain current density of 300μA/mm. For digital biasing we used the most unfavourable operating conditions: on-gate for n-type devices and off-gate for p-type devices.

3.2 Front Channel Threshold Shift

In Figs. 2 and 3 we have plotted the shift of the front channel threshold voltage as a function of the irradiation dose for PMOS and NMOS respectively. In '97 the transistors were measured directly after irradiation and after 2 months. At that time we observed a large increase of the threshold voltage for PMOS by about 550 mV. Now, for the enhanced technology the threshold voltage increases only by 115mV and 160 mV after 10Mrad and 20Mrad respectively. This shows that the technology has been improved.

For NMOS the shift is even smaller, -30mV, (-60mV) after 10Mrad, (20Mrad). In '97 we observed a positive

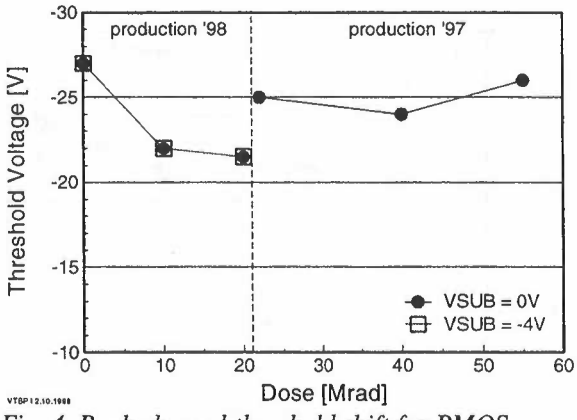


Fig. 4. Back channel threshold shift for PMOS

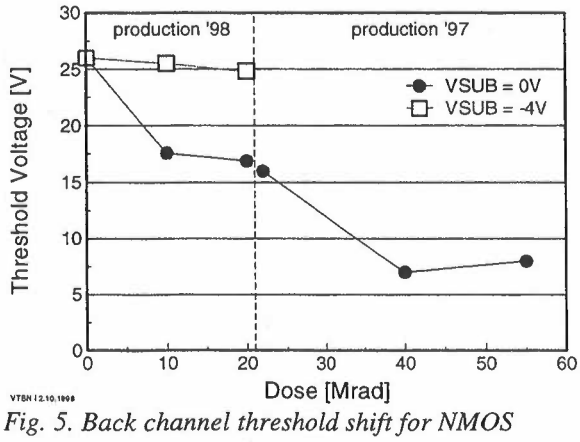


Fig. 5. Back channel threshold shift for NMOS

threshold voltage shift after irradiation. The discrepancy can be explained with postirradiation effects, namely annealing effects occurring within the 99 hours of the irradiation period. This tendency is also confirmed by the measurements which took place two months later, where the maximum threshold shift amounted to 130mV.

3.3 Back Channel Threshold Shift

Figs. 4 and 5 illustrate the back channel threshold voltage shift for PMOS and NMOS transistors as a function of total irradiation dose. We irradiated the devices with the back gate connected to 0V and to -4V. For PMOS in the new technology the threshold voltage decreases by about 5V independent of biasing during the irradiation. For the old technology the changes were negligible even when irradiated up to 55Mrad so that for PMOS devices this parameter is not critical.

For NMOS the back channel threshold decreases from 25V to about 17V after 10Mrad and 20Mrad, when irradiated with the back gate connected to 0V, but the changes are negligible when irradiated with the back gate connected to -4V. In '97 we observed a large decrease of the back channel threshold voltage to about 7V but even for the highest radiation dose, the back channel threshold is sufficiently high to prevent the transistor from malfunction. For all devices and for all irradiation doses we did not observe irradiation induced leakage current.

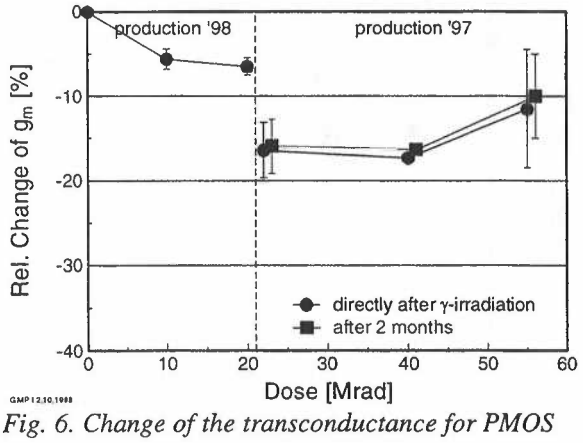


Fig. 6. Change of the transconductance for PMOS

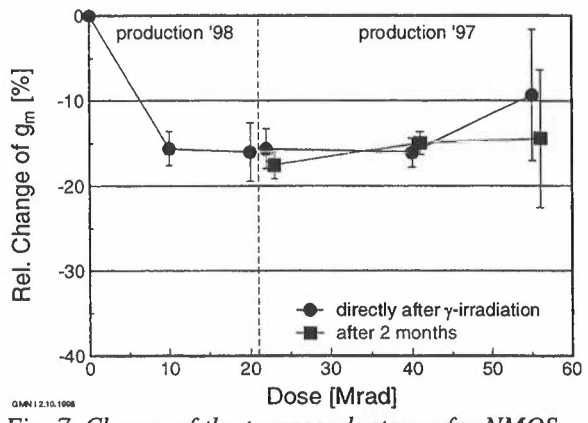


Fig. 7. Change of the transconductance for NMOS

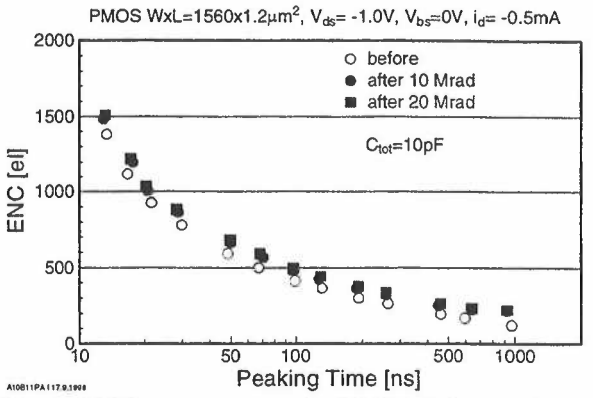


Fig. 8. ENC measurements for PMOS before and after 10 Mrad γ and 20 Mrad γ

3.3 Change of the Transconductance

From the DC measurements we have extracted the transconductance g_m. Figs. 6 and 7 show the change of the transconductance for PMOS and NMOS transistors measured at the drain current density of 1mA/mm and drain voltage V_{ds}=-1V (PMOS) and V_{ds}=1V (NMOS).

For the enhanced PMOS g_m decreases by 6% only after 10Mrad and 20Mrad. The NMOS transistor is more sensitive to gamma irradiation, its transconductance decreases by 16%.

3.4 Noise Behaviour

Fig. 8 shows the ENC measurements for PMOS with a gate width of 1500μm biased with the drain current of 500μA and loaded with the total input capacitance of 10pF. The open circles show the ENC before irradiation, the full circles the ENC after 10Mrad gamma irradiation and the full squares the ENC after 20Mrad gamma irradiation. We observe only a small degradation of the noise behaviour. Fits to the measurements show that the white serial noise increases by about 10% and that the serial 1/f noise contribution is not significant in the interesting range of peaking time (20ns ÷ 50ns). The total ENC increases by 10% at peaking time of 25ns.

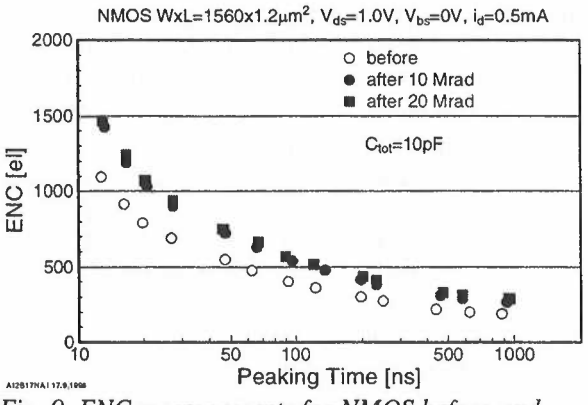


Fig. 9. ENC measurements for NMOS before and after 10 Mrad γ and 20 Mrad γ

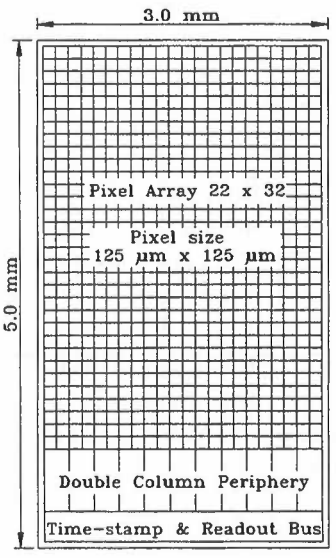


Fig. 11. Layout of the Pixel Readout Chip

In Figs. 9 we have plotted the ENC measurements before and after irradiation for a NMOS with the same gate width of 1500µm and for the same biasing and total input capacitance. The degradation of the noise behaviour is higher. The values of the power densities of each noise source extracted from a fit show that after the total dose of 20Mrad the white serial noise increases by a factor of 1.4 and the 1/f noise increases by a factor of 3. However, the total noise increases by 30% at a peaking time of 25ns. We also observe that there is no significant difference in noise behaviour and in the DC characteristics after 10Mrads and 20Mrad. It seems that radiation induced changes saturate at the latest after 10Mrad.

4. PIXEL READOUT ARCHITECTURE

Fig. 11 shows schematically the architecture of the chip we have translated from DMILL to the RICMOS IV process. The chip consists of 704 pixel cells organized in 11 double columns with 32 pixels in each column. The pixels have a 125µm x 125µm square shape. At the bottom of the chip the double column periphery and time stamps and buffers are located. The overall dimensions of the chip are 5mm by 3mm.

The main purpose of the chip is to implement and test the complete analogue block. The readout logic has a reduced circuit architecture and will be changed for the next generation of chips.

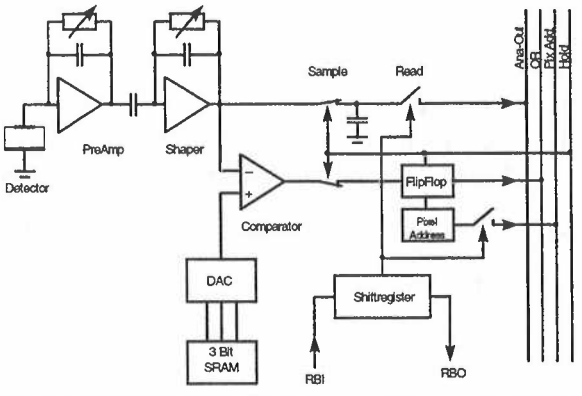


Fig. 12. Schematic block diagram of the pixel unit cell

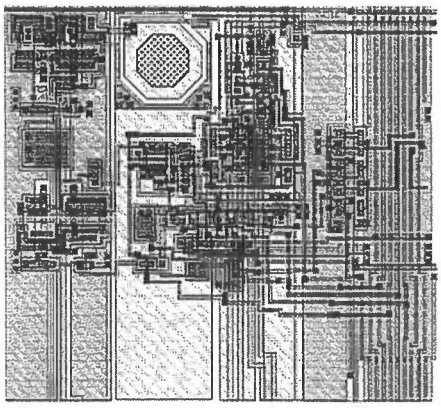


Fig. 13. Layout of the pixel unit cell in RICMOS IV technology

The main features of the architecture are:

- Each pixel is able to detect a hit and to store analogue and digital information.
- The pixels are organized in independent double columns. Information from the pixel cells is transmitted along a double column to logic at the end of the double column
- the double column periphery allows simultaneous readout and data taking by reading out only column pairs having at least one pixel hit.

The block diagram of the pixel unit cell is plotted in Fig. 12. Each pixel cell contains a preamplifier, shaper, comparator, flag register and shift register controlling the readout. The gain of the preamplifier as well as the time constant of the shaper is controlled by the feedback resistors. The shaper output is connected to a capacitance, which acts as an analogue store, and to the input of a comparator. The threshold of a the comparator is controlled by the 3 bit DAC to accommodate variations of the parameters of the transistors.

The double column periphery is equipped with control logic, which recognizes a hit in a pixel, a twelve-bit buffer for time stamping, and readout logic controlling the data transfer from pixels to the periphery.

5. PHYSICAL IMPLEMENTATION

Fig. 13 shows the layout of the pixel cell in RICMOS IV. The bump bonding pad is the most sensitive part of the pixel electronics since it is on the input of the preamplifier. It is placed asymmetrically in the pixel cell to reduce cross talk from the digital readout lines to the input of the preamplifier. The digital lines are placed in between pixel cells. The third metal layer is used to shield the pixel detector against transients on long digital lines, while the second layer is mainly used for power distribution. The active area consumption in RICMOS IV is 30% lower than in DMILL

Examples of the layout of the double column logic are presented in Fig. 14. Although the circuit is identical in both cases, the active area used to implement it is a factor of 2 higher in DMILL than in RICMOS IV. Another advantage is due to the availability of three metalization layers. We can completely abandon long polysilicon lines and improve the power distribution.

6. FIRST RESULTS

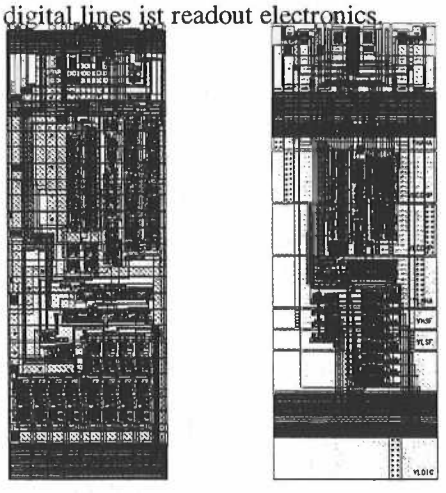
At the time of the workshop we have performed only some preliminary tests on pixel readout electronics. Fig. 15 shows the pulse at the shaper output for 6250 e^- injected to the pixel. The peaking time is less than 22ns for a power dissipation of 35μW. The picture is taken with a picoprobe attached to the shaper output which represents an additional capacitance of 25fF. The gain amounts to 3.9mV/100el.

Fig. 16 shows a threshold scan. Here we have plotted the detection efficiency as a function of the charge injected into the pixel. The slope of the curve is proportional to the noise. The typical noise is 70e^- (without detector at the input) for a threshold of about 1400e^-.

7. CONCLUSION

The threshold voltage and transconductance of the RICMOS IV transistors show low degradation and no increase of leakage current after irradiation with a total dose of 55Mrad (photons from Co^{60}).

The noise degradation after 20Mrad is low. It increases by 10% for PMOS and by 30% for NMOS. This demonstrates that the technology is fully suitable for electronics to be used in the LHC environment. The high transistor density and the availability of four metal layers are very advantageous because of better power distribution, lower area consumption, and better shielding of the pixel detector against transients on the digital lines ist readout electronics.



DMILL SOI RICMOS IV SOI

Fig. 14. Layout of the double column perifery in DMILL and in Honeywell processes.

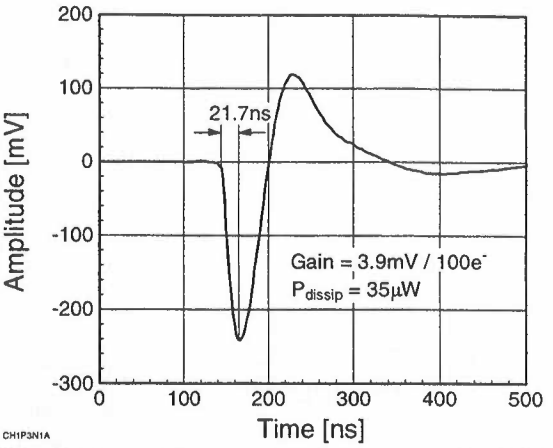


Fig. 15. Signal pulse at the shaper output for 6250e^- injected to the input.

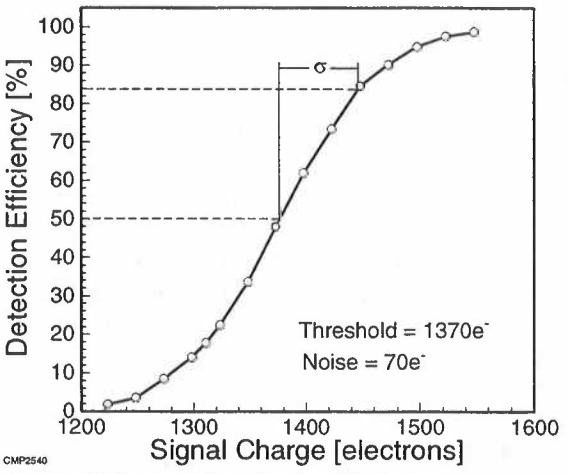


Fig. 16. Threshold scan indicating noise measurement.

8. ACKNOWLEDGEMENTS

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9. REFERENCES

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[2] S.T.Liu et al, Total dose Hard 0.8 Micron SOI CMOS Devices, Proceedings of the First Workshop on Electronics for LHC Experiments, pp 33-37, 1995